Digital Control of a PWM Switching Amplifier with Global Feedback

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ABSTRACT

A digitally controlled class-D amplifier using global feedback is presented. The output signal of the amplifier is sampled using a sigma-delta analogue-to-digital converter. A novel compensation strategy is used to minimize distortion resulting from ripple feedback of the output signal. An evaluation system, based on a Field Programmable Gate Array, was developed and an experimental evaluation was performed. State-of-the-art performance was achieved.

1. INTRODUCTION

Digital pulsewidth modulated (PWM) signals can be synthesized with high accuracy from the PCM audio input signal at relatively modest switching frequencies in the digital domain. However, the performance of open-loop digital switching amplifiers is limited by nonlinearities and other imperfections introduced by the MOSFET output stage and output filter. These nonlinearities include timing errors due to blanking time and current dependent delays of the switching transitions as well as amplitude errors resulting from the non-linear on-state resistance of the MOSFET switches, current dependent overshoot and variations in the power supply voltage. Another source of imperfection that is often overlooked is the low-pass output filter. This filter modifies the frequency response of the amplifier in a load dependent manner. It increases the amplifier’s output impedance and adds distortion due to the non-linear nature of the filter inductor.

Feedback provides an effective way to compensate all of the above-mentioned imperfections. To date digital feedback strategies for class-D amplifiers have mainly been based on local feedback loops [1]-[8], relying partly on the use of analogue circuitry to reduce the required resolution of the analogue-to-digital converter that samples the error signal. While the local feedback approach effectively compensates for the non-idealities of the output stage it provides no rejection of the imperfections associated with the output filter. The fact that the output filter modifies the frequency response of this type of amplifier is often overlooked.

This paper focuses on the digital closed-loop control of a switching amplifier using global feedback. A sigma-delta analogue-to-digital converter is used to sample the output voltage of the amplifier. A novel ripple compensation strategy is used to eliminate the effect of aliasing of the PWM signal resulting from ripple feedback. A simple way to characterise the load is presented.

2. OVERVIEW OF THE DIGITALLY-CONTROLLED AMPLIFIER

Fig. 1 shows an overall block diagram of the switching amplifier with global feedback. The overall structure of the feedback loop is a classical control loop in its simplest form. The output signal of the amplifier is sampled by an analogue-to-digital converter and subtracted from an up-sampled version of the 24-bit digital audio input signal. The resulting signal serves as input to a digital pulse width modulator. The power stage can either be a half-bridge or full-bridge converter.

Careful attention has to be paid to the choice of the analogue-to-digital converter. The most obvious requirement is that the analogue-to-digital converter must have noise and distortion specifications that exceed those put forward for the complete amplifier. Another requirement is the sampling rate of the analogue-to-digital converter. PWM results in groups of harmonics centred at integer multiples of the switching frequency. The magnitude of...
these harmonics shows a first order decrease with frequency. Since the LC low-pass filter is a second order filter a high sampling rate is required in order to avoid aliasing.

State-of-the-art multi-bit sigma-delta analogue-to-digital converters satisfy the requirements in terms of signal-to-noise ratio and sampling frequency. However, the long delays associated with the digital low-pass FIR filters used to remove the shaped quantization noise in this type of converter poses a significant challenge in terms of the design of the control loop. The solution is to use the modulator output of the sigma-delta AD converter and to substitute a minimum-phase IIR filter for the linear-phase FIR filter. In a perfectly linear system the shaped high-frequency quantization noise would remain above the audio band. However, due to the sampling nature of the pulse width modulator some of the quantization noise is aliased into the audio band [11] and additional digital filtering is required to lower the quantization noise to acceptable levels. The quality of the multi bit DA converter in the sigma-delta AD converter is critical, since its linearity determines the overall performance of the amplifier [9].

3. RIPPLE COMPENSATION

It is well-known that feedback of the ripple signal present on the output voltage of a PWM amplifier causes a non linearity in the PWM process due to aliasing of the high-frequency carrier components [11], [13]. This causes distortion of the output signal of the amplifier, even if the output stage is considered to be perfect. A detailed analysis of the distortion caused by this phenomenon was carried out in [11] under the assumption that the input signal to the amplifier is constant. Two distortion mechanisms were identified. The first mechanism is distortion of the pulse width which causes a DC non linearity. The second, more subtle distortion mechanism is related to a signal dependent non-linear time shift of the PWM pulses (phase modulation).

In [11] a class of minimum aliasing error loop filters are presented that obtains minimum distortion due to the use of quadrature sampling. A different approach to solving the ripple feedback problem (with a single integrator as loop filter) is presented in [13]. The carrier signal is modulated by a small-amplitude signal which is proportional to the derivative of the input signal. In [14] a remarkably simple solution to the ripple feedback problem was presented by cancelling the unmodulated edge in a single-sided modulator. This section further investigates this compensation strategy and shows how it can be extended to the current system.

First consider the simplified naturally-sampled single sided PWM feedback loop, with loop filter $G(s)$, shown in Fig. 2. The waveforms describing the operation of this circuit over a segment of the input signal $i(t)$ are shown in Fig. 3. The feedback signal is taken directly from the

Fig. 1: Overall schematic of the switching amplifier with global feedback.
modulator output \( p(t) \). The sawtooth carrier \( s(t) \) is added to \( p(t) \), thereby cancelling the unmodulated edge \( p(t) \). The resulting signal \( y(t) \) is a ‘sawtooth-like’ waveform of which the time average (calculated over one switching period) is equal to that of the modulator output \( p(t) \).

The advantage of this ripple compensation technique lies in the observation that shape of the ripple component of \( y(t) \) and hence \( x(t) \) is largely independent of the duty cycle \( \pi(t) \).

Signal \( y(t) \) is subtracted from the audio input signal \( i(t) \) and passed through the loop filter \( G(s) \). The loop filter typically consists of a chain of integrators with high gain throughout the audio band and less than unity gain at the switching frequency. Fig. 3 shows the output signal \( x(t) \) of a typical loop filter. Since the control loop accurately tracks the input signal \( x(t) \), the crossings of \( x(t) \) and the sawtooth carrier \( s(t) \) coincide with those of \( i(t) \) and \( s(t) \). It can again be observed that the shape of the ripple component of \( x(t) \) is independent of the average value of \( x(t) \), thereby significantly reducing the nonlinearity resulting from the interaction of the ripple component of the PWM input signal and the pulse width modulation process.

In order to quantify the advantages of this ripple compensation strategy the DC-linearity of the pulsewidth modulator in the presence of the modified ripple signal is investigated. Consider the feedback loop of Fig. 2 in the case where \( i(t) \) is constant (DC input signal). Fig. 4 illustrates the operation of the pulsewidth modulator in the presence of the modified ripple feedback signal. The difference \( \Delta x \) between the average modulator input \( \pi(t) \) and the average modulator output \( \pi(t) \) provides a quantitative measure of the non-linearity of the pulse width modulation process in the presence of the ripple signal. Now consider the ripple component

\[
\Delta x = x(t) - \pi(t)
\]

of \( x(t) \). This ripple component is the response of the loop filter \( G(s) \) to a time-shifted replica of the sawtooth carrier \( s(t) \). Furthermore, \( \Delta x \) is equal to the minimum value \( r_{\min} \) of \( r(t) \). Since changes in the average modulator input only affects the phase of \( r(t) \), \( \Delta x \) is independent of the average modulator input signal. This shows that the DC
non-linearity of the pulsewidth modulator has been reduced to a simple DC-offset. The value of this DC-offset only depends on properties of the loop filter and is independent of the average modulator input signal. This DC offset is easily compensated by the feedback loop.

The next step is to show how the ripple compensation technique of Fig. 2 can be extended to the switching amplifier that includes a low-pass LC filter, like that of Fig. 1. Fig. 5 shows three equivalent implementations of the ripple compensation strategy. For the moment the MOSFET output stage is considered to be ideal and is represented by a gain, denoted by \( A \). For a full-bridge output stage this gain is equal to the DC-bus voltage \( V_{d} \), while \( A = \frac{V_{d}}{2} \) for a half-bridge output stage.

Figs. 2 and 5(a) are essentially equivalent in terms of ripple feedback, the only difference being that the ripple component only passes through \( G(s) \) in Fig. 2 while it passes through the series combination of \( F(s) \) and \( G(s) \) in Fig. 5(a). A direct application of Fig. 5(a) is impractical since it would require adding an amplified version of the sawtooth carrier to the output voltage of the power stage before the low-pass LC filter.

Figs. 5(b) and (c) are derived from Fig. 5(a) through simple block diagram manipulation. In Fig. 5(b) the sawtooth carrier is passed through a filter of which the transfer function is identical to that of the low pass LC filter before being subtracted from \( w(t) \). It should be noted that in a practical system the frequency response of the LC filter at and above the switching frequency is relatively independent of the load resistance. As a result the ripple compensation technique is relatively insensitive to the exact matching of LC filter’s transfer function. Fig. 5(c) shows that the ripple compensation technique is equivalent to pre-distortion of the sawtooth carrier. In a digital implementation this pre-distortion can be done off-line and the resulting carrier stored in a lookup table.

4. DESIGN OF THE DIGITAL LOOP FILTER

Fig. 6 shows a \( z \)-domain block diagram of the feedback loop. The low-pass LC filter has been transformed to the \( z \)-domain. The digital pulse width modulator is assumed to be a linear component, with noise source \( N_1(z) \) representing the quantization noise associated the finite bit length of the pulse width modulator. However, it should be kept in mind that the pulse width modulation process suffers from fold-back distortion. As a result high frequency noise in \( X(z) \) may fold back into the audio band.

The gain of the output stage is again represented by \( A \), while any imperfection in the output stage are modelled by error source \( E(z) \). The sigma-delta analogue-to-digital converter is represented by its closed-loop transfer function \( H(z) \), which includes the transfer function of the analogue-anti aliasing filter. For practical purposes it can be assumed that the analogue-to-digital can be modelled by a single sample delay \( H(z) = z^{-1} \). Noise source \( N_2(z) \) represents the shaped quantization noise of the sigma-delta modulator. The ripple compensation strategy of Fig. 5(b) was used in the prototype design since this implementation doesn’t require recalulation of the ripple compensation lookup table when making changes to \( G_2(z) \) or \( G_3(z) \).

The digital loop filter consists of three sections. The first, denoted by \( G_1(z) \) in Fig. 6 provides digital cancellation of the poles of the low-pass LC filter by placing two zeros at the location of these poles. Exact cancellation of the LC filters poles isn’t necessarily required. However, in order to ensure a stable control loop, two zeros would have to be placed in the vicinity of these two poles. It also contains two high-frequency poles to attenuate the quantization noise of the analogue-to-digital converter. The second section, denoted by \( G_2(z) \) is a low pass filter. The aim of this filter is to attenuate the quantization noise of the analogue-to-digital converter. The third section denoted \( G_3(z) \) consists of a chain of integrators with feed forward summation and local resonator feedback loops [16], p177. This section provides the required gain across the audio band.

The ability of the control loop to reject imperfections in the output stage and LC filter is described by the transfer function

\[
R(z) = \frac{V_d(z)}{E(z)} = \frac{F(z)}{1 + H(z)G(z)F(z)},
\]

where

\[
G(z) = G_1(z)G_2(z)G_3(z).
\]

Furthermore, the transfer function describing the ability of the control loop to attenuate the quantization noise \( N_1(z) \) of the digital pulse width modulator is described by:

\[
NTF_1(z) = \frac{V_d(z)}{N_1(z)} = \frac{AF(z)}{1 + H(z)G(z)F(z)}
\]

Since both \( F(z) \approx 1 \) and \( H(z) \approx 1 \) throughout the audio band, the key to a successful design lies in ensuring that \( G(z) \) has high gain throughout the audio band.
The shaped quantization noise $N_2(z)$ of the analogue-to-digital converter also requires some consideration. The prototype design made use of a commercial sigma-delta analogue-to-digital converter [15]. This analogue-to-digital converter was operated at a sampling frequency of 19.6608 MHz. According to [15], Fig. 41 the noise floor of this sigma-delta AD converter is more or less flat up to 1.5 MHz. It rises by approximately 60 dB at half the clock frequency. As mentioned above, excessive levels of high-frequency noise at the input of the pulse width modulator results in fold back distortion or may even cause instability of the feedback loop.

To summarize, a number of factors have to be taken into account when designing the loop filter:

- The feedback loop should have high enough open-loop gain throughout the audio band to shape the quantization noise of the digital pulse width modulator and suppress errors resulting from imperfections in the output stage.
- The cut-off frequency $\omega_c$ of the LC low-pass filter is usually selected to be significantly lower than the...
switching frequency. The two zeros of $G_1(z)$ that cancel these poles causes a second order rise in the magnitude of the open-loop transfer function

$$NTF_2(z) = \frac{X(z)}{N_2(z)} = G(z)$$

above $\omega_c$. This gives rise to the amplification of the quantization noise $N_2(z)$ of the analogue-to-digital converter, resulting in fold-back distortion. A possible solution to this problem is to place a lead compensator in the analogue domain. In the implementation that is described in this paper it is possible to overcome this problem through careful design of the digital loop filter without additional analogue circuitry. However, a commercial system would use an analogue to digital converter with much more out-of-band noise in which case an analogue lead compensator would be required.

- Additional digital low-pass filtering is required to attenuate the quantization noise of the analogue-to-digital converter. However, placing the poles associated with this filter near the audio band leads to instability of the control loop.

- The stability of the control loop is also dependent on the proper implementation of the ripple compensation method described in the previous section. The experimental system proved to be unstable without proper ripple compensation.

Finding the optimal trade-off between these requirements requires careful sculpting of the transfer function of the digital loop filter.

A switching frequency of 768 kHz was selected for the experimental system and the low-pass LC-filter has a cut-off frequency of 70 kHz. The digital feedback loop is clocked at 19.6608 MHz, except for the 7-bit digital pulse width modulator which operates at a clock frequency of 98.304 MHz. The input signal $X(z)$ of this modulator is thus updated at every fifth clock cycle of the 98.304 MHz clock. During the experimental evaluation it was found that this 5:1 clock ratio didn’t cause measurable distortion in the audio band as long as sufficient analog low-pass filtering (which the LC filter provides) was included before the analog-to-digital converter.
As second order noise shaping loop with noise transfer function

$$NTF_3(z) = (1 - z^{-1})^2$$ (4)

(as described in [17]) was placed around the pulselwidth modulator. The intersection between the sawtooth carrier and the input signal of the pulse width modulator is detected and the noise shaper is only clocked at this intersection. In this way the noise shaper is clocked at the switching frequency of 768 kHz.

Fig. 7 shows the (open loop) Bode plot of $G_1(z)G_2(z)G_3(z)F(z)$. $G_3(z)$ consists of a chain of five integrators with feed forward summation and local resonator feedback loops. One of the five poles are located at 1 in the $z$-plane, while the other poles pairs are located at 11.3 kHz and 18.6 kHz on the unit circle. The associated zeros are placed at 31.2 kHz and 41.6 kHz with damping ratios of 0.214 and 0.39, respectively.

The poles of the LC-filter are cancelled by the zeros of $G_1(z)$, while the poles of $G_1(z)$ are placed at 700 kHz to attenuate the quantization noise of the analogue-to-digital converter. The second section, denoted by $G_2(z)$ is a second order Chebyshev type I filter with a cut-off frequency of 1 MHz and pass band ripple of 10 dB. An additional four-cycle delay (203 ns) was also included in $G(z)$ when analyzing the stability of the control loop. This accounts for delays resulting from the gate drivers, analogue-to-digital converter and digital pulse width modulator. The resulting control loop is stable with a gain margin of -4.41 dB and a phase margin of 31.7 degrees.

Fig. 8 shows a bode plot of transfer function $NTF_2(z)$ as defined in equation 3. The second order rise in this transfer function above 70 kHz is a result of the zeros of $G_1(z)$, as described earlier. The poles of $G_1(z)$ and the low-pass filter $G_2(z)$ provide sufficient attenuation of the high-frequency quantization noise of the analogue-to-digital converter to prevent fold back distortion.

A load sensitivity analysis was performed to investigate the stability of the control loop under different load impedances. The load impedance affects the location of the poles of the LC low-pass filter. The sensitivity analysis showed that when placing the zeros of $G_1(z)$ to cancel the poles of the LC filter with a 4 Ω resistive load, the control loop would be stable for load resistances ranging from 2.6 Ω to 35 Ω. However, as pointed out earlier, low distortion of the output voltage as well as stable operation also depends on accurate ripple compensation.

The following section describes a simple method to characterize the load and select the parameters of $G_1(z)$ to ensure stability as well as optimal performance with a variety of different loads.

5. LOAD CHARACTERIZATION

A simple method, based on measuring the impulse response of the LC filter and load, was selected for load characterization. Since the practical system was based on an FPGA the emphasis was on simplicity of implementation rather than minimizing the required number of clock cycles.
The output stage generates an impulse of one switching cycle. The output voltage is measured by the sigma-delta analogue-to-digital converter. It was assumed that the output filter and load can be described by a second-order model. Although a real-world loudspeaker presents a higher-order system, this approach proved to perform well in the experimental system. The impulse response is measured when the amplifier is turned on.

The measured (time domain) impulse response \( y_m(n) \) is compared with a number of simulated impulse responses which were pre-calculated for different values of the load resistance. These simulated impulse responses can be stored in lookup tables. The sum of the absolute values of the residuals

\[
S = \sum_{n=1}^{N} |y_m(n) - y_s(n)|
\]

serves as a cost function to determine the best match.

Fig. 9 shows the measured and best-matching simulated impulse responses for a 8 \( \Omega \) load.

While other time-domain system identification techniques, like the least squares optimization technique, typically rely on more sophisticated numerical methods to minimize the cost function \( S \), this simple method is robust and can easily be implemented in an FPGA while placing low demands on the device resources.

6. EXPERIMENTAL RESULTS

An experimental system was constructed to evaluate the control strategy. The experimental system is based on the EP3C25 Cyclone III FPGA from Altera. A commercial integrated digital audio receiver and asynchronous sample rate converter up samples the incoming 24-bit digital audio signal to 196.61 kHz. A sixth order polynomial up sampler then up samples the digital audio signal to 19.6608 MHz, which is the sampling frequency of the sigma-delta analogue-to-digital converter. The digital pulse-width modulator operated at a clock frequency of 98.304 MHz and a switching frequency of 768 kHz was selected, as mentioned earlier.

The FPGA was programmed in VHDL. One channel consumed 28% of the FPGA’s logic elements, 7% of the dedicated logic registers and 100% of the embedded multipliers. The load characterisation, as described in the previous section, was done off-line using Matlab and has not yet been implemented in VHDL.

Apart from the standard anti-aliasing filter described in [15] a simple resistive divider was the only additional analogue component in the feedback path. The full-bridge outputs stage was operated at a DC-bus voltage of 25 V. All measurements were preformed with an Aux-0025 low-pass filter and a 20 kHz AES17 filter.

Fig. 10 shows the spectrum of the output voltage with a 1 kHz full-scale input signal and an 8 \( \Omega \) load.

Fig. 10 shows the spectrum of the output voltage with a 1 kHz full-scale input signal and an 8 \( \Omega \) load. The measured THD plus noise is 0.0009% at 15 W. This compares favourably with the THD plus noise of high-performance digital-to-analogue converters.
Fig. 11: Spectrum with a two-tone input with an 8 Ω load.

Fig. 11 shows the spectrum of the output voltage with a two-tone input at 17 and 18 kHz. The THD plus noise as a function of frequency with a full-scale input signal is depicted in Fig. 12. The sharp peaks at 10.5 kHz are due to large second order harmonics at 21 kHz which fall outside the audio band.

Fig. 12: THD plus noise as a function of frequency with a full-scale input signal.

The frequency response of the amplifier for 8 Ω and 4 Ω loads are shown in Fig. 13. The frequency response is flat to within 0.1 dB across the audio band.

Fig. 13: Frequency response with a full-scale input signal.

Figs. 14 and 15 shows the THD plus noise as a function of power for 8 Ω and 4 Ω loads, respectively.

Fig. 14: THD plus noise with a 8 Ω load.

7. CONCLUSIONS

A digital control strategy with global feedback was presented to increase the performance of digitally controlled class-D amplifiers. State-of-the-art performance was achieved with a THD plus noise of 0.0009% at 15 W. The amplifier has a flat frequency response and low distortion across its operating range of frequency and power.
A novel ripple compensation technique and a simple method to characterise the load was presented.

8. REFERENCES


Fig. 15: THD plus noise with a 4 Ω load.