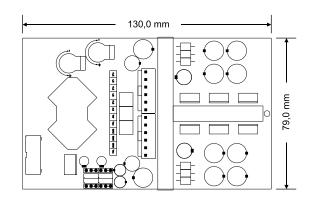
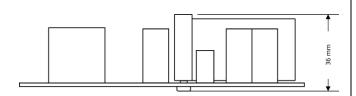


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High Efficiency Power Amplifier Module (LZ, OEM version)





Highlights

- Flat, fully load-independent frequency response
- Low output impedance
- Very low, frequency-independent THD
- Very low noise
- Fully passive loop control
- Consistent top performer in listening trials
- Short term 1200W@2R capable

Features

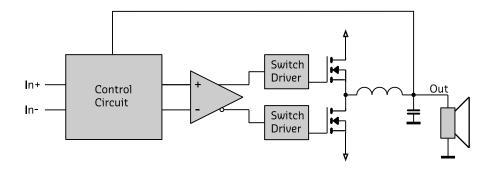
- Runs on unregulated +/- rails
- Pop-free start and stop control
- Differential audio input
- Overcurrent, overvoltage and over temperature protection
- Weight: 250gms

Applications

- Monitor loudspeakers for recording and mastering studios
- Audiophile power amplifiers for professional and consumer use
- Public Address systems
- Home theatre systems
- Active loudspeakers

Description

The UcD700LZ(OEM version) amplifier module is a self-contained high-performance class D amplifier intended for a wide range of audio applications, ranging from Public Address systems to ultrahigh-fidelity replay systems for studio and home use. Chief distinguishing features are flat frequency response irrespective of load impedance, nearly frequency-independent distortion behaviour and very low radiated and conducted EMI. Control is based on a phase-shift controlled self-oscillating loop taking feedback only at the speaker output.







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1 Performance data

Power supply = \pm /-85V, Load= \pm 0, MBW= \pm 40kHz, unless otherwise noted

Power supprig - +7-65V, coud-412, MBW-40KH2, unless otherwise noted										
ltem	Symbol	Min	Тур	Max	Unit	Notes				
Output Power	P _R	-	1200	-	W	THD=1%, Load=2Ω ¹⁾				
		-	700	-	W	THD=1%, Load=4Ω				
		-	440	-	W	THD=1%, Load=8Ω				
Distortion	THD+N	-	-	0.02	%	20 Hz <f<<math>20kHz²⁾ Pout<$P_R/2$</f<<math>				
		-	-	0.005	%	20Hz <f<20khz, pout="1W</td"></f<20khz,>				
DC offset	V_{DC}	-	-	5m	V					
Output noise	U _N	-	30μ	35μ	V	Unwtd, 20Hz-20kHz				
Output Impedance	Z _{out}	-	-	20m	Ω	f<1kHz				
	33.	-	-	150m	Ω	f<20kHz				
Power Bandwidth	PBW		20-35k		Hz	3)				
Frequency Response		10	-	50k	Hz	+0/-3dB. All loads				
Voltage Gain	$A_{V,tot}$	25.5	26	26.5	dB					
Voltage Gain	$A_{v,tot}$	12.5	13	13.5	dB	Input buffer bypassed				
Required input level for 700W/4Ω/THD=1%			2.65		V	Appropriate supply voltage level assumed				
Ripple Rejection	PSRR		65		dB	Either rail, all frequencies				
						•				
Efficiency	η		92		%	Full power				
Idle Losses	P ₀		15		W	+/- 90V rails				
Standby Current	I _{STBY}		10m		Α					
Current Limit	I _{OUT,P}		38		Α	Hiccup mode after 40 ms				

Note 1: Heatsink construction does not allow for long term maximum power output in 2Ω . A continuous maximum power output of $350W/2\Omega$ (when sufficiently cooled) should be maintained. **Note 2:** At higher audio frequencies there are not enough harmonics left in the audio band to make a meaningful THD measurement. High frequency distortion is therefore determined using a 18.5 kHz + 19.5 kHz 1:1 two-tone IMD test.

Note 3: Dielectric losses in the output capacitor limit long term (>30s) full-power bandwidth to 15kHz.

2 Audio Input Characteristics

Item	Symbol	Min	Тур	Max	Unit	Notes
Input Impedance	Z _{IN}		100k		Ω	Either input to ground
Input Imp. (buffer bypassed)	Z _{IN}		1.8k		Ω	Either input to ground
Common Mode Rejection Ratio	CMRR		75		dB	All frequencies





3 Absolute maximum ratings

Correct operation at these limits is not guaranteed. Operation beyond these limits may result in irreversible damage

resart in inteversible damage									
Item	Symbol	Rating	Unit	Notes					
Power supply voltage	V _B	+/-100	V	Unit shuts down when either rail exceeds 96V					
Driver supply voltage	V_{DR}	+16	V	Referenced to -V _B . Vdr current is 200mA Max ¹⁾					
Audio Input voltage	V _{IN}	+/-12	V	Either input referenced to ground					
Aux. supply voltage	V _{AUX}	+/-15	V						
Peak output current	I _{OUT,P}		Α	Unit current-limits at 38 A					
Air Temperature	T _{AMB}	65	°C						
Heat-sink temperature	T _{SINK}	90	°C	insure this condition under most adverse use ²⁾					

Note 1: Amplifier is disabled when VDR drops below 13V.

Note 2: Overtemperature protection kicks in at a heatsink temperature of 100 °C.

4 Recommended Operating Conditions

Item	Symbol	Min	Тур	Max	Unit	Notes
Power supply voltage	V _B	75 ¹⁾	90	95 ²⁾	V	
Driver supply voltage	V _{DR}		15		V	
Load impedance	Z _{LOAD}	1			Ω	
Source impedance	Z_{SRC}			7k	Ω	
Effective power supply	C _{SUP}	10m ³⁾			F	Per rail, per attached
storage Capacitance						amplifier. 4Ω load.

Note 1: Reduced performance.

Note 2: Unit shuts down when either rail exceeds 96V.

Note 3: The effective power supply storage capacitance of Hypex SMPS is already in excess of $10.000\mu F$. Do not add supplementary capacitance.

5 Connections

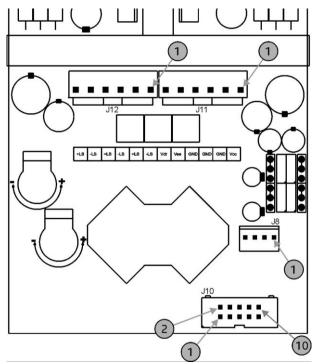


Figure 1: Connector pinning UcD700LZ (OEM version).





5.1 J8/J10: Auxiliary connection.

J8 Connector type: 4-pin MOLEX® KK® series, part number 22-27-2041.

J10 Connector type: Standard 2.54mm boxheader.

Pin (J8)	Pin (J10)	Function
4 ¹⁾	7	Non inverting Audio Input
3 ¹⁾	3	GND
2 ¹⁾	8	Inverting Audio Input
1 ¹⁾	6	ON/OFF control
	10	DC error detection
	9	Current limiter monitoring
	5	Clipping detection
	4	Amplifier ready
	1	+12V ²⁾
	2	-12V ²⁾

Note 1: This connector is primarily intended for use in prototyping and the connections are paralleled with J10. It is recommended to use J10 for all connections including signal in the final product.

Note 2: This auxiliary supply only supplies the on-board buffer opamp and can be omitted when this opamp is bypassed.

5.2 J11: power supply connection.

Connector type: JST (www.jst.com) B6P-VH. Matching cable part: VHR-6N

Pin	Туре	Function
1, Vcc	Input	Positive power supply connection
2, 3, 4, GND	Input	Power supply ground connection
5, Vee	Input	Negative power supply connection
6, Vdr	Input	Driver supply connection, VDR (referenced to Vee)

5.3 J12: Loudspeaker output

Connector type: JST (www.jst.com) B6P-VH. Matching cable part: VHR-6N

Commeden type	Service test (www.jst.com) ser vini i laterini g easte part. Vinit ett								
Pin	Type	Function							
1, 3, 5, LS-	Output	Output (cold)							
2, 4, 6, LS+	Output	Output (hot)							

5.4 Clipping Detection Characteristics

The UcD700LZ (OEM version) has an integrated output clipping detection which will pull pin J10:5 low in case of such an event.

Item	Min	Тур	Max	Unit	Notes
Voltage on pin J10:5, clipping			1	V	Internal open collector 1)

Note 1: Must be pulled to a positive voltage by means of an external resistor. Open collector maximum output current: 100mA. Maximum collector voltage: 65V.





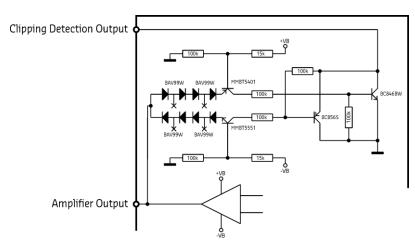


Figure 2: Clipping Detection Output interface.





5.5 DC-Error Detection Characteristics

The UcD700LZ (OEM version) has an integrated DC-error detection which will pull pin J10:10 low in case of such an event. It is recommended to sense this fault condition and to interrupt both power supply lines in such an event.

Item	Min	Тур	Max	Unit	Notes
Voltage on pin J10:10, DC-error			1	V	Internal open collector 1)

Note 1: Must be pulled to a positive voltage by means of an external resistor. Open collector maximum output current: 100mA. Maximum collector voltage: 150V.

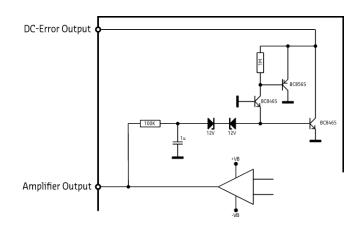


Figure 3: DC-Error Output interface.

5.6 Amplifier ON/OFF Characteristics

The UcD700LZ (OEM version) is enabled by pulling pin J10:6 (or J8:1) low. Leaving this pins floating will put the amplifier in standby.

Iten	1		Min	Тур	Max	Unit	Notes
Volt	age on pin J10:6/J8:1, lef	t floating			6,5	V	Internally pulled up 1)

Note 1: Must be pulled low by means of an open collector.

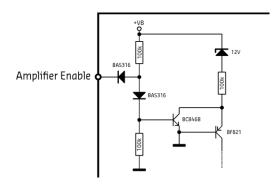


Figure 4: Amplifier On/Off Control interface.

5.7 Amplifier Ready Characteristics

The UcD700LZ (OEM version) has an integrated Amplifier Ready condition which will pull pin J10:4 high to indicate that the amplifier shut itself down due to an error. This error can be either an overvoltage event or a shorted output.

Item	Min	Тур	Max	Unit	Notes
Voltage on pin J10:4, error			5,6	V	Internally pulled up





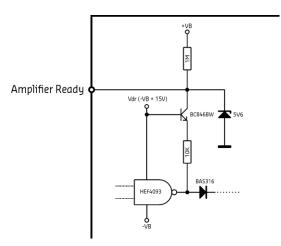


Figure 5: Amplifier Ready Output interface.

5.8 Current Limiter Monitoring

The UcD700LZ (OEM version) has a current limiter monitoring output which is pulled low in the event of an output current limiting situation. This is output is not latched/delayed and is therefore only active when the limiter is active.

Item	Min	Тур	Max	Unit	Notes
Voltage on J10:9, Current limiting	-0,7			V	Internally pulled up

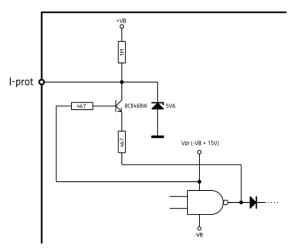


Figure 6: Current limiter monitoring.

5.9 Amplifier start-up delay

During initial power up the amplifier is disabled for approx. 1.5s regardless of the state of the Amplifier Enable pin. Once powered up there is no start or stop delay. The Amplifier Ready pin remains high during the initial power up.

5.10 Thermal protection

When the heatsink reaches a temperature of $100 \, ^{\circ}$ C the amplifier is automatically disabled. Once the temperature is back at a safe level (<100 $^{\circ}$ C) the amplifier is enabled again.





5.11 Signal path characteristics



The UcD700LZ (OEM version) enables the user to choose between two different ways of input signal routing. Standard jumper settings are set to use the on-board buffer opamp (NE5532). In order to bypass the on-board buffer and AC-coupling capacitors all four jumpers (J1, J2, J4, J5) need to be set according to picture.

Note: Since the amplifier is now fully DC-coupled the user must ensure that the input signal is completely free of DC components.

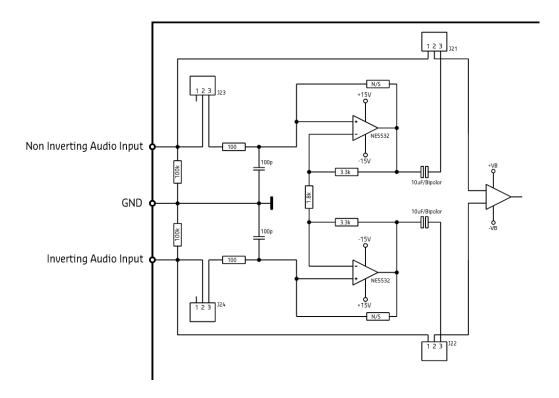


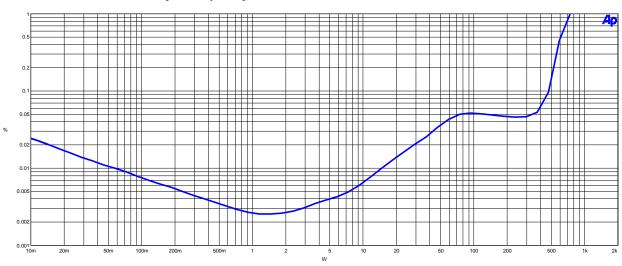
Figure 7: Audio Input Buffer interface.



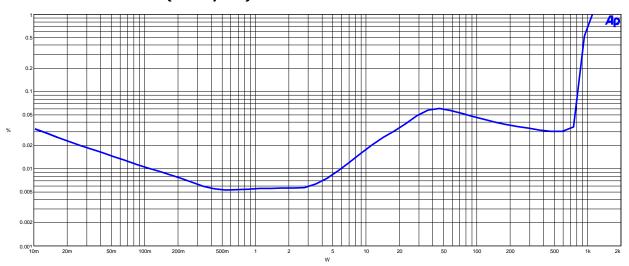


6 Typical Performance Graphs

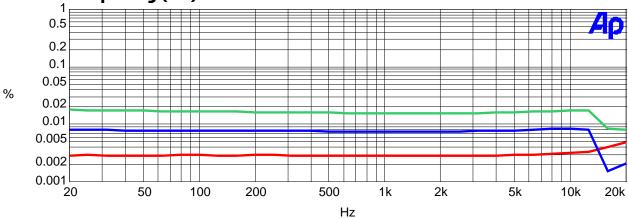
6.1 THD vs. Power (1kHz, 4Ω)



6.2 THD vs. Power (1kHz, 2Ω)



THD vs. Frequency (8 Ω)

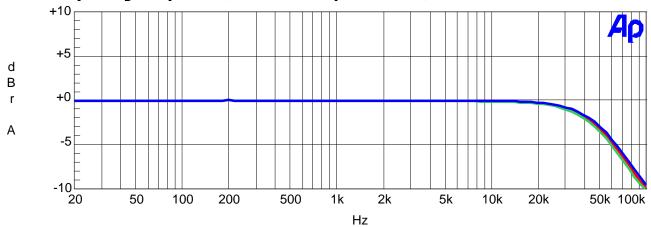


From top to bottom: 40W, 10W, 1W



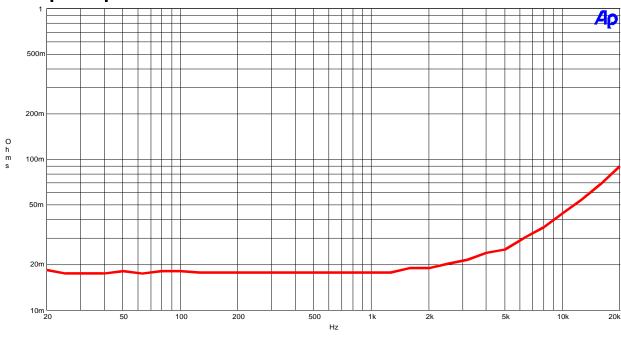


6.3 Frequency Response (4Ω , 8Ω and open circuit)

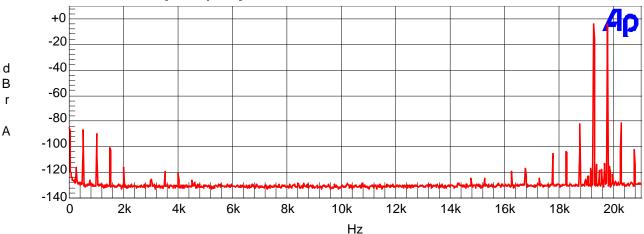


From top to bottom: open circuit, 8Ω , 4Ω

6.4 Output Impedance



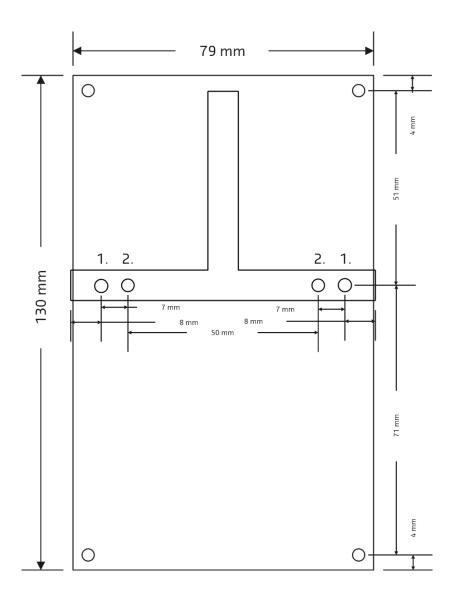
6.5 19+20kHz IMD (10W, 4Ω)







7 Connection diagram



- 1. UNC 8-32
- 2. Metric M4





DISCLAIMER: This subassembly is designed for use in music reproduction equipment only. No representations are made as to fitness for other uses. Except where noted otherwise any specifications given pertain to this subassembly only. Responsibility for verifying the performance, safety, reliability and compliance with legal standards of end products using this subassembly falls to the manufacturer of said end product.

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Document Revision	PCB Version	Description	Date
R1	UcD700LZ0EM V1	Initial Draft.	15.03.2010
R2	UcD700LZ0EM V1	VDR UVLO spec added.	11.10.2010
R3	UcD700LZ0EM V1	Idle losses corrected	09.05.2011
R4	UcD700LZOEM V1	Recommended operating conditions updated	25.05.2012
R5	UcD700LZOEM V1	Format changed	17.01.2013