

# DSA254

## ▼ MULTICHANNEL CLASS D AMPLIFIERS

### ▼ DSA254

#### ▶ DATASHEET

## Introduction

The options are endless with the ability of a classic 4 x 250W single ended setup, a power-packed performance of 2 x 500W, or the enhanced capability of a parallel-bridge-tied load configuration of 1 x 1000W and the ability of driving 2Ω, 4Ω, 8Ω and 70V-100V speakers.

DSA254 OEM adapts to your distinct audio preferences for any loudspeaker configuration.

## Key features

- 1Ch, 2Ch, 3Ch and 4Ch configurable
- 70V/100V Compatible
- NCOREx Technology
- I<sup>2</sup>C Compatible
- Single Header Wireless Design

## Key Specifications

Output Power	1000W Total
THD+N	0.001%
Frequency response	51kHz
Output Noise	18μV
Signal To Noise Ratio	124dB
Idle Power (85V, Low Idle Setting)	9W

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# 1 Safety Precautions



This module operates at high voltages and carries hazardous voltages at accessible parts. These parts may never be exposed to inadvertent touch. Observe extreme care during installation and never touch any part of the unit while it is connected to the mains.

Allow all capacitors to discharge for 10 minutes before handling it.



Attention: Observe precautions for handling electrostatic sensitive devices. This module uses semiconductors that can be damaged by electrostatic discharge (ESD).

Damage due to inappropriate handling is not covered by warranty. This product has no user-serviceable parts.



Ce module est sous tension secteur et certaines de ses pièces accessibles sont sous une tension dangereuse. Ces pièces doivent dans tous les cas être protégées contre contacts accidentels. Lors de l'installation, une prudence extrême s'impose. Ne jamais toucher les pièces du module quand celui-ci est relié au secteur. Isoler l'appareil du secteur et attendre 10 minutes pour laisser à tous les condensateurs le temps de se décharger avant de le manipuler.

secteur. Isoler l'appareil du secteur et attendre 10 minutes pour laisser à tous les condensateurs le temps de se décharger avant de le manipuler.



Attention : Respecter les consignes de sécurité pour la manipulation d'appareils sensibles aux courants électrostatiques. Ce module est pourvu de semi-conducteurs qui peuvent être endommagés par les décharges électrostatiques (DES).

Les dommages causés par un usage non approprié sont exclus de la garantie. Ce produit ne contient aucune pièce devant être entretenue par l'utilisateur.

1. Read these instructions.
2. Keep these instructions.
3. Heed all warnings.
4. Follow all instructions.
5. Do not use this apparatus near water.
6. Only use attachments/accessories specified or approved by the manufacturer.
7. Refer all servicing to qualified service personnel. Servicing is required when the apparatus has been damaged in any way, liquid has been spilled or objects have fallen into the apparatus, the apparatus has been exposed to rain or moisture, does not operate normally or has been dropped.
8. Don't run any cables across the top or the bottom of the module. Apply fixtures to cables to ensure that this is not compromised.
9. Observe a minimum clearance of 3mm with all possible conducting parts (housing etc.).
10. Natural convection should not be impeded by covering the module (apart from the end applications housing).
11. Before using this product, ensure all cables are correctly connected and the power cables are not damaged. If you detect any damage, do not use the product.
12. Changes or modifications not expressly approved by Hypex Electronics will void compliance and therefore the user's authority to operate the equipment.
13. Service or modifications by any person or persons other than by Hypex Electronics authorized personnel voids the warranty.

## 2 Electrical Specifications

### 2.1 Recommended Operating Conditions & Supply Currents

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Note
Input Voltage Main	Symmetric supply (+/-)	$V_{MAIN}$	35	63	90	V	1)
Input Current Main	Idle operation	$I_{MAIN}$		79		mA	
Input Current Main	Full Power			10		A	
Input Voltage Vaux	Symmetric supply (+/-)	$V_{AUX}$	15	15	25	V	
Input Current Vaux		$I_{AUX}$		65	100	mA	
VSBY		$V_{UC}$	5	5	25	V	4)
ISBY		$I_{UC}$	1	7.5	10	mA	2)
External Driver Supply Voltage		$V_{DR}$	15	15	19	V	1, 3)
External Driver Supply Current		$I_{DR}$		200	250	mA	

**Note 1:** Over Voltage Protection (OVP) is triggered if allowable range is exceeded.

**Note 2:** The maximum current largely depends on current draw by user-side IO.

**Note 3:** Floating and referenced to HV-.

**Note 4:** This optional supply voltage enables user to keep the microcontroller 'alive' when the rest of the system is shut down.

### 2.2 Absolute Maximum Ratings

**Correct operation at these limits is not guaranteed. Operation beyond these limits may result in irreversible damage.**

Parameter	Conditions	Symbol	Min	Max	Unit	Note
Input Voltage Main	Symmetric supply (+/-)	HV+/-	-100	100	V	
VDR Supply Voltage		$V_{DR}$		25	V	
Vaux Supply Voltage		$V_{AUX}$		25	V	
Peak Output Current	Guarded by current limit at 14A	$I_{OUT,P}$		14	A	
Signal Input Voltage	Either input referenced to ground	$V_{IN}$		10	V	
IO Voltage			-0.3	3.6	V	
IO Current			-10	10	mA	
Collector Voltage	Open collector outputs when high	$V_{OC}$		25	V	
Collector Current	Open collector outputs when low	$I_{OC}$		2	mA	

### 2.3 Protection Limits

Parameter	Symbol	Max	Unit	Note
HV Undervoltage Lockout	$HV_{UVLO}$	35	V	
HV Overvoltage Lockout	$HV_{OVLO}$	98	V	
VDR Undervoltage Lockout	$VDR_{UVLO}$	14.5	V	
VDR Overvoltage Lockout	$VDR_{OVLO}$	20	V	
Overtemperature		105	°C	
Overtemperature lower hysteresis		95	°C	

## 2.4 Amplifier Specifications

### 2.4.1 Typical amplifier specifications

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Note
Distortion	20Hz<f<20kHz, 4Ω, P <sub>out</sub> <P <sub>r</sub> /2	THD+N	-	0.001	0.005	%	
CMRR	f<1kHz		50	75	-	dB	
Signal-To-Noise Ratio	1W	SNR	-	100	-	dB	
	250W	SNR		124		dB	
Output noise		V <sub>N</sub>	-	18	-	μV	
Output Impedance	f<20kHz	Z <sub>OUT</sub>	-	7	-	mΩ	
	f<1kHz	Z <sub>OUT</sub>	0.6	-	1.2	mΩ	
Frequency Response	+0/-3dB. All loads		-	51	-	kHz	
	+0/-0.3dB. All loads		-	31	-	kHz	
Voltage Gain		A <sub>V</sub>	-	20	-	dB	
Supply Ripple Rejection	f<1kHz	PSRR	-	75	-	dB	
Output Offset Voltage		V <sub>ool</sub>			30	mV	
Efficiency	Full power			85		%	
Output Current Limit		I <sub>OUT</sub>	10.5	12	13	A <sub>PK</sub>	
Idle Losses	+/- 46V	P <sub>O, Low</sub>	-	3.6	-	W	
		P <sub>O, High</sub>	-	6.7	-	W	
	+/- 63V	P <sub>O, Low</sub>	-	5.5	-	W	
		P <sub>O, High</sub>	-	10.5	-	W	
	+/- 84V	P <sub>O, Low</sub>	-	9	-	W	
		P <sub>O, High</sub>	-	16.5	-	W	

### 2.4.2 Amplifier Output Power (+/- 63V)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Note
Peak Output Power	1kHz, THD=1%, Single Ended Mode (SE)	P <sub>R, 4Ω</sub>	-	250	-	W	
		P <sub>R, 8Ω</sub>	-	200	-	W	
Peak Output Power	1kHz, THD=1%, Bridge Mode (BTL)	P <sub>R, 4Ω</sub>	-	300	-	W	
		P <sub>R, 8Ω</sub>	-	600	-	W	
		70V	-	350	450	W	
Peak Output Power	1kHz, THD=1%, Parallel Mode (PTL)	P <sub>R, 2Ω</sub>	-	700	-	W	
		P <sub>R, 4Ω</sub>	-	400	-	W	
		P <sub>R, 8Ω</sub>		200	-	W	
Peak Output Power	1kHz, THD=1%, Parallel Bridge Mode (PBTL)	P <sub>R, 4Ω</sub>	-	1000	-	W	
		P <sub>R, 8Ω</sub>	-	750	-	W	
		70V	-	700	900	W	

### 2.4.3 Amplifier Output Power (+/- 84V)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Note
Peak Output Power	1kHz, THD=1%, Single Ended Mode (SE)	$P_{R, 4\Omega}$	-	250	-	W	
		$P_{R, 8\Omega}$	-	400	-	W	
Peak Output Power	1kHz, THD=1%, Bridge Mode (BTL)	$P_{R, 8\Omega}$	-	600	-	W	
		$P_{R, 16\Omega}$	-	700	-	W	
		70V	-	350	450	W	
		100V	-	500	625	W	
Peak Output Power	1kHz, THD=1%, Parallel Mode (PTL)	$P_{R, 4\Omega}$	-	800	-	W	
		$P_{R, 8\Omega}$	-	400	-	W	
Peak Output Power	1kHz, THD=1%, Parallel Bridge Mode (PBTl)	$P_{R, 4\Omega}$	-	1000	-	W	
		$P_{R, 8\Omega}$	-	1450	-	W	
		70V	-	700	900	W	
		100V		1000	1250	W	

- Notes:**
- An Audio Precision AES17 20 kHz is used during this measurement.
  - Dielectric losses in the output capacitor limit long term (>30s) full-power bandwidth to 5kHz
  - See 7 Applications for connection methods
  - Output power per channel (4 x SE, 2x BTL/PTL, 1 PBTl)

## 3 Audio IO Specifications

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Note
DM Input Impedance		$Z_{IN,DM}$		4,8		k $\Omega$	
Source Impedance	Differential	$Z_{SRC}$			50	$\Omega$	
Load Impedance Range		$Z_{L,SE}$	1	4	-	$\Omega$	
		$Z_{L,BTL}$	2	8		$\Omega$	
		$Z_{L,PTL}$	1	2		$\Omega$	
		$Z_{L,PBTl}$	1	4		$\Omega$	

### 3.1 Audio Input

The INH/INC inputs form a differential pair. Note that the unbuffered input impedance is fairly low meaning that minimalist discrete circuits or valve input stages won't work. All op amps commonly used in audio can handle them though. Do not drive the input with fully floating sources, be it electrically floating ones like line driver IC's intended for driving XLR outputs or transformers. Using a floating source will always result in a common mode component that will exceed the common mode input range and will manifest itself as gross distortion. Make sure to set the outputs of your distortion analyser to grounded, not floating.

#### Signal Coupling

To achieve optimal signal coupling, the audio signal inputs are all DC coupled. One must make sure that the connected application is free of DC offset.

## 3.2 Application Considerations

### 3.2.1 Cooling

DSA254 might be an efficient Class D design, please bear in mind it has only the size of a smartphone. Demanding output power requirements require solid cooling solutions.

Use two M3 bolts to fasten the DSA254 to a heatspreader or heatsink. The 3mm holes in the heatsink are unthreaded enabling fastening from either top or bottom. Multichannel designs may require forced cooling.

Defects caused by overheating due to poor thermal management are not covered by warranty.

## 4 Environmental Specifications

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Note
Ambient temperature	Storage		-25		70	°C	
	Operation	$T_{AMB}$	0		65	°C	
Heatsink Temperature		$T_{H,MAX}$			90	°C	1)
Humidity	Max 85 percent relative humidity, non-condensing.						

**Note 1:** Thermistor limited. User to select heat sink to insure this condition under most adverse use case.

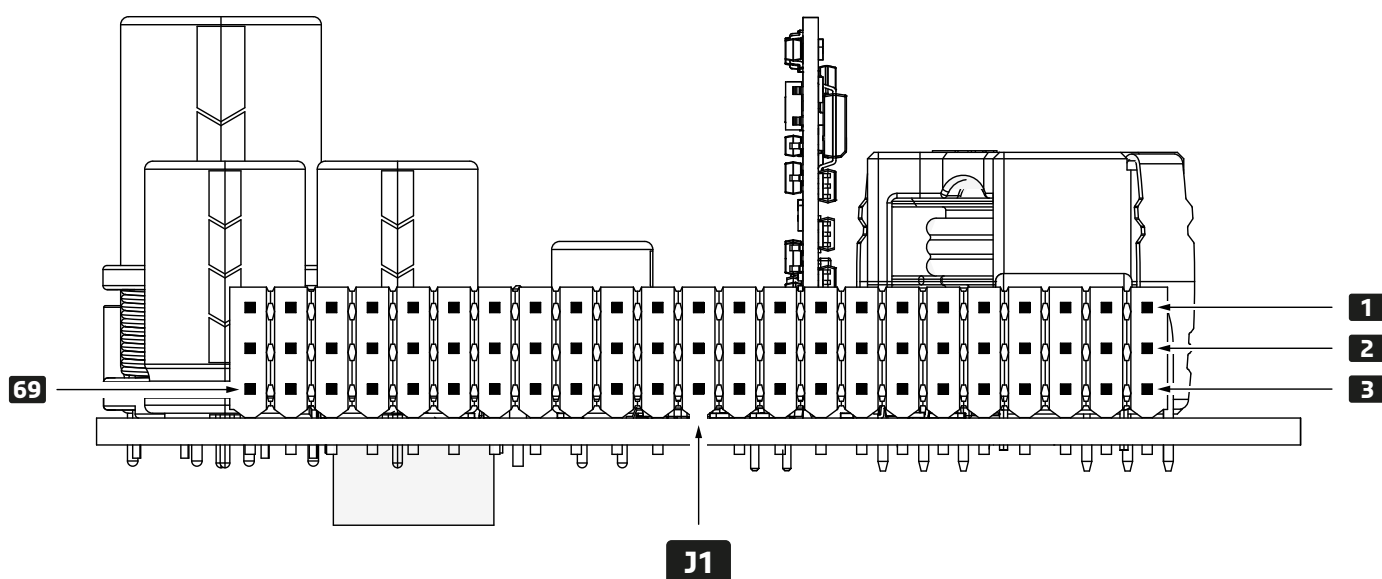
## 5 Connector Pinout

### J1 - Interface Connector

Pin	Direction	Function	Remarks
1, 2, 3	Output	CH4 OUT -	CH4 Cold Loudspeaker Output
4, 5, 6	Output	CH4 OUT +	CH4 Hot Loudspeaker Output
7, 8, 9	Output	CH3 OUT -	CH3 Cold Loudspeaker Output
10, 11, 12	Output	CH3 OUT +	CH3 Hot Loudspeaker Output
13, 14, 15	Output	CH2 OUT -	CH2 Cold Loudspeaker Output
16, 17, 18	Output	CH2 OUT +	CH2 Hot Loudspeaker Output
19, 20, 21	Output	CH1 OUT -	CH1 Cold Loudspeaker Output
22, 23, 24	Output	CH1 OUT +	CH1 Hot Loudspeaker Output
25	Input	GND	Ground
26	Input	VSBY	Standby Power Supply Input
27	Input	VAUX-	Negative Auxiliary Power Supply Input
28	Input	VAUX+	Positive Auxiliary Power Supply Input
29	Input	CH4 IN -	CH4 Inverting Audio Input
30	Input	CH4 IN +	CH4 Non-Inverting Audio Input
31	Input	CH3 IN -	CH3 Inverting Audio Input
32	Input	CH3 IN +	CH3 Non-Inverting Audio Input
33	Input	CH2 IN -	CH2 Inverting Audio Input
34	Input	CH2 IN +	CH2 Non-Inverting Audio Input
35	Input	CH1 IN -	CH1 Inverting Audio Input
36	Input	CH1 IN +	CH1 Non-Inverting Audio Input
37	Input	I <sup>2</sup> C ADDRESS	I <sup>2</sup> C Address
38		I <sup>2</sup> C SCL	I <sup>2</sup> C Clock
39		I <sup>2</sup> C SDA	I <sup>2</sup> C Data
40	Output	nFATAL	Catastrophic Fault Indication
41	Input	nPOWER GOOD	Power Good Amp
42	Output	nAMP RDY	Amp Ready
43	Input	MUTE CH3CH4	CH3 & CH4 Enable
44	Input	MUTE CH1CH2	CH1 & CH2 Enable
45	Output	nTMP WRN 2	Very High Temperature Indication (Either Channel)
46	Output	nTMP WRN 1	High Temperature Indication (Either Channel)
47	Input	nHPP CH3CH4	CH3 & CH4 Parallel Mode
48	Input	nHPP CH1CH2	CH1 & CH2 Parallel Mode
49	Output	nCLP CH1CH2	CH1 And/Or CH2 Clip Indicator
50	Output	nCLP CH3CH4	CH3 And/Or CH4 Clip Indicator



Pin	Direction	Function	Remarks
51	Input	Idle Adj	Idle Adjust Override
52	Input	VDR+	External driver supply connection, referenced to HV-
53	-	GND	Ground
54	-	NC	Not Connected
55, 56, 57, 59, 60	Input	HV-	Negative Main Power Supply
58, 61, 62, 63, 64	-	GND	Power Ground
65, 66, 67, 68, 69	Input	HV+	Positive Main Power Supply



67	64	61	58	55	52	49	46	43	40	37	34	31	28	25	22	19	16	13	10	7	4	1
HV+	GND	GND	GND	HV-	VDR+	nCLP CH1 CH2	nTMP WRN 1	MUTE CH3 CH4	nFTL	I2C ADD	CH2 IN +	CH3 IN -	VAUX +	GND	CH1 OUT +	CH1 OUT -	CH2 OUT +	CH2 OUT -	CH3 OUT +	CH3 OUT -	CH4 OUT +	CH4 OUT -
68	65	62	59	56	53	50	47	44	41	38	35	32	29	26	23	20	17	14	11	8	5	2
HV+	HV+	GND	HV-	HV-	GND	nCLP CH3 CH4	nHPP CH3 CH4	MUTE CH1 CH2	nPWR GD	I2C SCL	CH1 IN -	CH3 IN +	CH4 IN -	VSBY	CH1 OUT +	CH1 OUT -	CH2 OUT +	CH2 OUT -	CH3 OUT +	CH3 OUT -	CH4 OUT +	CH4 OUT -
69	66	63	60	57	54	51	48	45	42	39	36	33	30	27	24	21	18	15	12	9	6	3
HV+	HV+	GND	HV-	HV-	NC	Idle Adj Ovr	nHPP CH1 CH2	nTMP WRN 2	nAMP RDY	I2C SDA	CH1 IN +	CH2 IN -	CH4 IN +	VAUX -	CH1 OUT +	CH1 OUT -	CH2 OUT +	CH2 OUT -	CH3 OUT +	CH3 OUT -	CH4 OUT +	CH4 OUT -

## 6 IO Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Logical High Input Voltage	$V_{IH}$	2.65		3.6	V	1)
Logical Low Input Voltage	$V_{IL}$	-0.3		0.5	V	
Logical Low Output Voltage	$V_{OL}$		0.7		V	

**Note 1:** Internally pulled up to 3v3, except I<sup>2</sup>C SCL and I<sup>2</sup>C SDA

### 6.1 Operation In Hardware And Software Mode.

The user can freely choose between hardware and software mode. No jumper settings are required. If a parameter is set in hardware mode, it must first be reset in hardware mode before it can be operated in software mode, and vice versa.

#### 6.1.1 Address Selection

The DSA supports up to 16 I<sup>2</sup>C addresses. Set the address by pulling the I<sup>2</sup>C Address to GND through a resistor.

Pull-down resistor at Pin 31	Dec I <sup>2</sup> C address	Binary I <sup>2</sup> C address
0	88	1011000x
1.8k	89	1011001x
3.9k	90	1011010x
6.8k	91	1011011x
10k	92	1011100x
12k	93	1011101x
18k	94	1011110x
22k	95	1011111x
27k	96	1100000x
33k	97	1100001x
47k	98	1100010x
56k	99	1100011x
82k	100	1100100x
120k	101	1100101x
180k	102	1100110x
390k	103	1100111x

x = r/w bit

#### 6.1.2 I<sup>2</sup>C Registers

Register 0: Module General commands/status			
Bit	Function	R/W	Description
0	AllAmpEnable	R/W	Enable all amplifiers
1	Reserved	R/W	
2	Reserved	R/W	
3	Reserved	R/W	
4	Reserved	R/W	
5	AmpReady	R	Amplifier is enabled and ready
6	AmpError	R	An Error occurred on one or more amplifiers
7	SupplyError	R	

### Register 1: Read-only module supply status

Bit	Function	R/W	Description
0	VDROver	R	VDR overvoltage
1	VDRUnder	R	VDR undervoltage
2	PosHVOver	R	Positive HV overvoltage
3	PosHVUnder	R	Positive HV undervoltage
4	NegHVOver	R	Negative HV overvoltage
5	NegHVUnder	R	Negative HV undervoltage
6	VauxError	R	Vaux undervoltage not present
7	HVDiff	R	Positive HV / Negative HV difference too high

### Remaining module registers

Register	Function	R/W	Description
2	PosHV	R	Positive HV voltage reading
3	NegHV	R	Negative HV voltage reading
4	VDR	R	VDR voltage reading
5	Reserved	R	
6	Reserved	R	
7	ProductCode	R	Product code
8	Version	R	Firmware version
9	Build	R	Firmware build

Registers 2 and 3 represent an unsigned byte-value and return a positive number between 0 and 250. For example: a value 76 corresponds with 76Volt.

Register 4 also represent an unsigned byte-value and return a positive number between 0 and 250, but that value needs to be divided by 10. For example: a value of 214 corresponds with 21.4Volt. Note that for register 4 a value of 214 would correspond with a value of 21.4V (as it represents VDR).

### Register 10: Amp1 control commands

Bit	Function	R/W	Description
0	AmpEnable	R/W	Enable
1	OverruledIdleCurrent	R/W	User controlled idle setting
2	OverruledIdleLevel	R/W	Setting idle current
3	OverrulePPCH12	R/W	User controlled parallel power
4	ParallelPowerCH12	R/W	Current PP setting
5	Reserved	R/W	
6	Reserved	R/W	
7	Reserved	R/W	

### Register 11: Amp1 status

Bit	Function	R/W	Description
0	AmpReady	R	Ready
1	Failure/DCErr	R	Catastrophic failure detected
2	Sustained Overload	R	Sustained overload detected
3	Overload Pending	R	Short term overload detected
4	OTP	R	Over temperature
5	ClipIndication	R	Clip indication
6	IdleCurrentLevel	R	Current status (high idle, low idle)
7	Reserved	R	

### Register 12: Amp1 temperature

Temperature (°C)	Register value (bin)	Register value (dec)
-10	11110110	246
-9	11110111	247
-8	11111000	248
-7	11111001	249
-6	11111010	250
-5	11111011	251
-4	11111100	252
-3	11111101	253
-2	11111110	254
-1	11111111	255
0	00000000	0
1	00000001	1
2	00000010	2
3	00000011	3
4	00000100	4
5	00000101	5
6	00000110	6
7	00000111	7
8	00001000	8
9	00001001	9
Etcetera		

Register 12 represent a signed 8-bit value as a temperature. It is coded as 2's-complement in the range of -10°C .. 125°C.

Channel Specific I <sup>2</sup> C Registers				
Amp#	Amp# Control	Amp# Status	Amp# Temperature	Reserved
1	10	11	12	13
2	14	15	16	17
3	18	19	20	21
4	22	23	24	25

Only Amp 1 registers are depicted. Amp-specific registers 10, 11, 12 (and 13) are repeated for all 4 amplifier channels, as is shown in the table above.

### 6.1.3 I<sup>2</sup>C Pins

Pin 38 is configured as SCL and pin 39 as SDA. These lines should be pulled to 3.3V with 4.7k resistors externally. The I<sup>2</sup>C bus should be operated at the standard 100kHz rate. Please make sure the I<sup>2</sup>C bus to this amplifier is isolated from other I<sup>2</sup>C buses, in order to prevent an I<sup>2</sup>C bus hangup when the supply for the amplifier is turned off.

## 6.2 Supply Connections

A symmetrical supply must be connected to the HV-, GND and HV+ pins. The amplifier will operate from the minimum voltage mentioned in Section '2.1' upward but rated output power is not available at low voltages. The floating VDR supply should be connected between HV- and VDR. Any other connection may cause damage or excessive heat output. The VDR supply's negative pin should be connected to HV- as close to the DSA254 amplifier as possible.

All GND pins are directly connected to the same ground plane. A GND pin (25) is provided near the small-signal end of the connector for convenience only. No distinction is made between "signal ground" and "power ground" because both inputs and outputs are configured as differential signal pairs that do not rely on GND as a reference potential.

## 6.3 VSBY

This pin can be used to keep the Microcontroller powered while the rest of the system is not.

## 6.4 nFATAL

nFATAL is an open drain, active low output which is asserted when the amplifier senses a large DC voltage at the output. When a >13V DC potential is detected nFATAL is pulled low to indicate catastrophic failure. After unmuting a channel, this option is disabled for 200ms to allow the amplifier to start up.

**IMPORTANT:** For safety reasons, the application must be able to respond to this line by turning the power supply off.

Do not use output relays. Apart from causing distortion, a relay is not suited to disconnect a heavily inductive load like a loudspeaker. Typical loudspeakers store enough energy to weld the relay shut, maintaining the safety hazard.

## 6.5 nPower Good

This signal can be used by a power supply to indicate that it is ready to deliver power. If not used, this pin should be tied to ground. The amplifier can start after this pin has been low for at least 3 seconds and if all its power requirements are met. If this pin is pulled high or left floating, the amplifier is muted.

## 6.6 nAMP RDY

The nAMP RDY pin is an open drain output that is pulled low whenever the amplifier is amplifying audio. When it mutes, for whatever reason, nAMP RDY goes high. This includes periodic mutes after sustained overcurrent events.

## 6.7 MUTE

Pulling the nENA CH1CH2 or nENA CH3CH4 input pin low enables the respective amplifier channels. Leaving the pins open mutes the channels.

## 6.8 nTMP WRN

“These open drain output pins are pulled low to indicate temperature warnings. A temperature warning is generated when one or multiple amplifier channels exceed a threshold temperature. These threshold values are:

- nTMP WRN1: 100 °C
- nTMP WRN2: 115 °C

If nTMP WRN2 is triggered, the amplifier’s channels get muted until all amplifier channel temperatures are below 105 °C

## 6.9 nHPP

Pulling this input pin low enables Parallel Power mode, synchronising the respective channels’ power stages. This is required when connecting CH1/CH2 or CH3/CH4 in parallel. When operating in CH1/CH2 in Parallel Power mode only the input of CH1 needs to be driven. When operating in CH3/CH3 in Parallel Power mode only the input of CH3 needs to be driven. Beware that the outputs of the parallel amplifier channels need to be connected in parallel electrically if this mode is used.

## 6.10 nCLP

The nCLP CH1CH2 and nCLP CH3CH4 indicator pins are active low, open collector outputs, meaning that the nCLP indicator of several channels may be paralleled. These signals are internally pulled up to 3V3, but an external pull-up resistor may also be applied, pulling the pin up to 25V max. The nCLP indicator is asserted whenever the amplifier is unable to track the input accurately:

- Normal clipping
- Current limiting
- Signal input during mute

Note that whilst muted the amplifier is clearly unable to track any input other than zero. The application circuit should ignore the nCLP flag during mute as it is likely that the nCLP indicator will be chattering most of the time.

## 6.11 Idle Adj

The Idle Adj pin allows the user to change the amplifier’s idle current. The pin has three defined conditions:

- Open: Automatic mode
- Pulled down through 10k: Force high idle
- Pulled down to GND: Force low idle

In automatic mode the amplifier chooses its own idle setting based on the voltage applied between the HV+/HV- rails. The amplifier starts in high idle mode. It switches to low idle mode above 130V between HV+ and HV-. Below 120V the amplifier switches back to high idle mode.

In force high idle mode, the amplifier always uses its highest idle current setting. In force low idle mode, the amplifier always uses its lowest idle current setting.

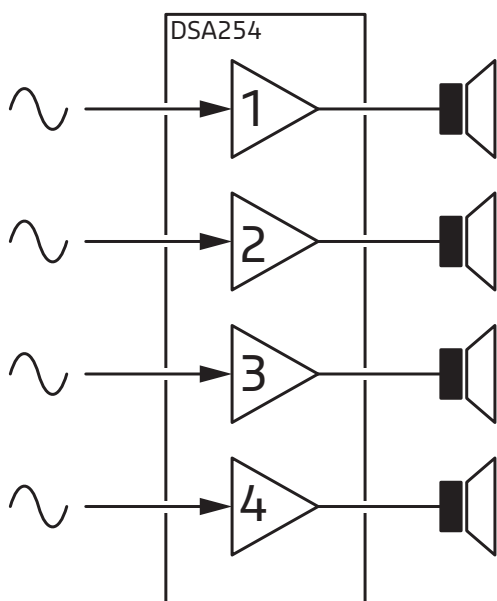
The lower idle setting reduces the energy dissipated by the amplifier, which is especially beneficial for multi-channel systems in small enclosures or when using a high supply voltage.

The higher idle setting draws more energy but yields better THD results.

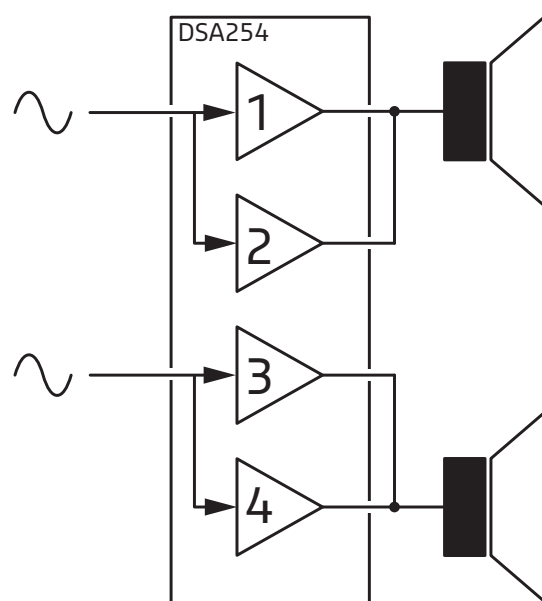
## 7 Applications

The DSA254 can be configured in almost any way imaginable:

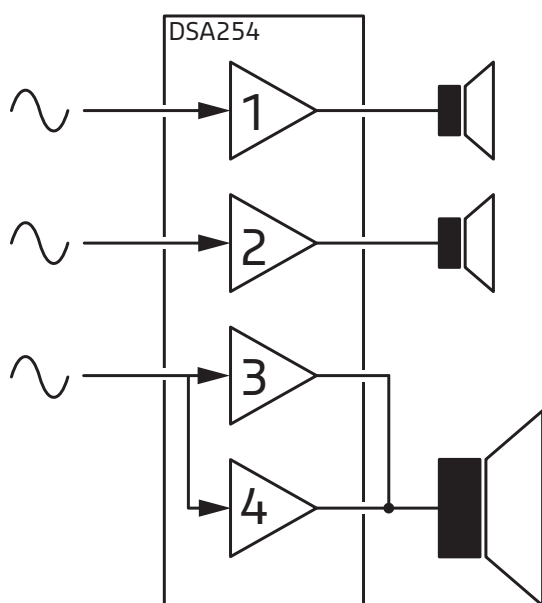
Please note that 70V/100V applications require two channels to be bridged.



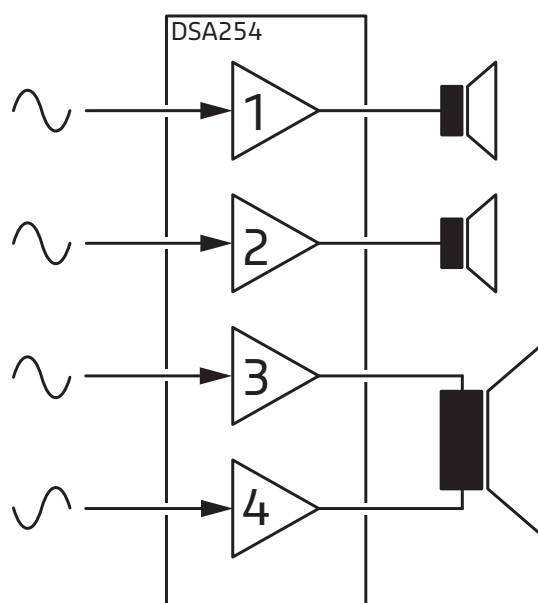
4 channel - Single Ended mode



2 channel - Parallel Power mode <sup>1</sup>

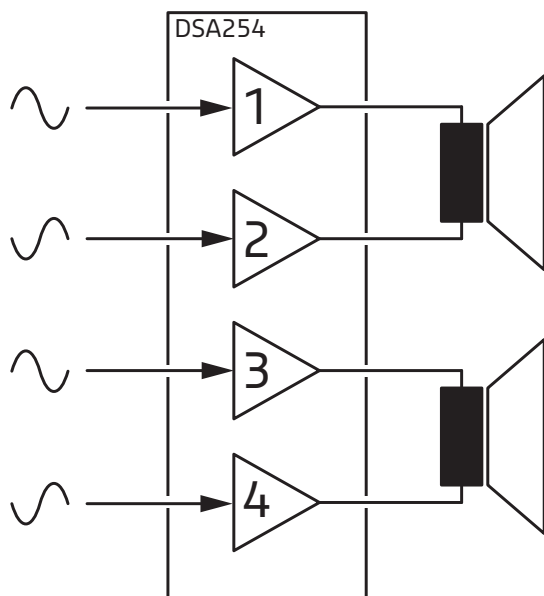


3 channel - Single Ended / Parallel Power mode <sup>1</sup>

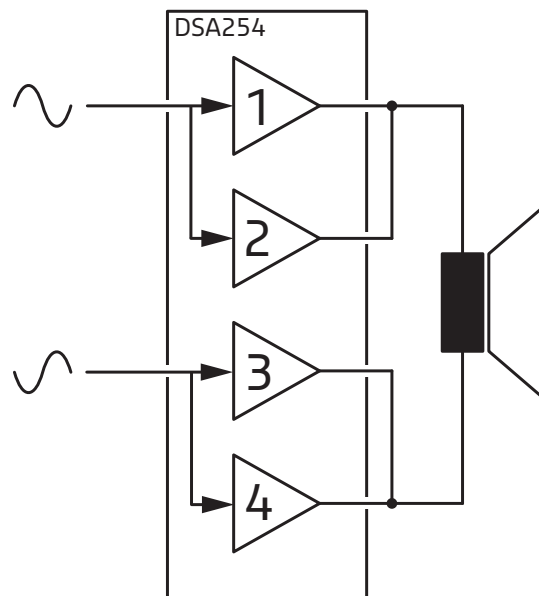


3 channel - 2 x Single Ended + 1 x BTL mode

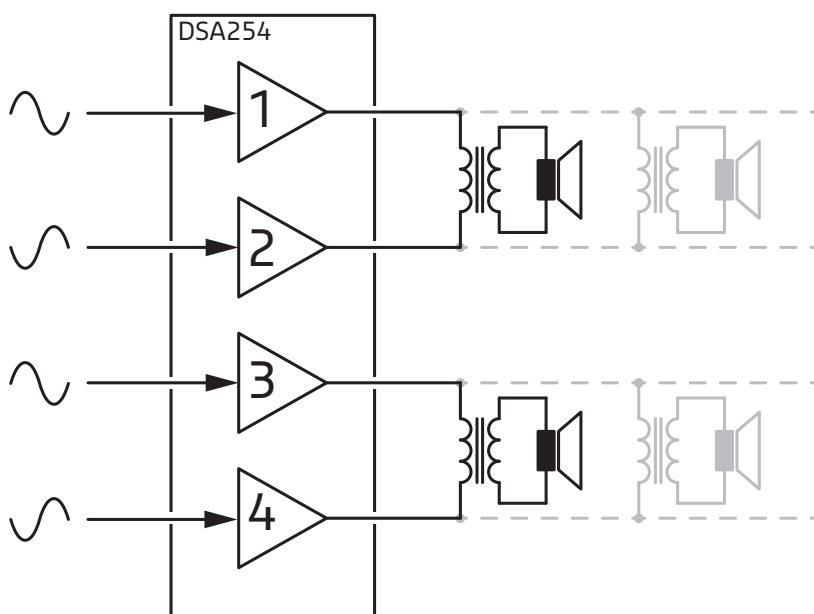
**Note 1:** To use this mode, either Parallel Power control bits or nHPP pins must be set and the channels' outputs must be connected in parallel electrically.



2 channel - BTL Mode



1 channel - PBTL Mode <sup>1</sup>



2 channel - 70V/100V mode

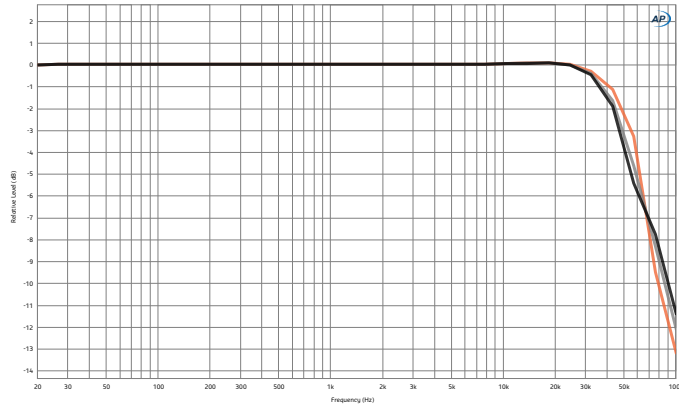
**Note 1:** To use this mode, either Parallel Power control bits or nHPP pins must be set and the channels' outputs must be connected in parallel electrically.



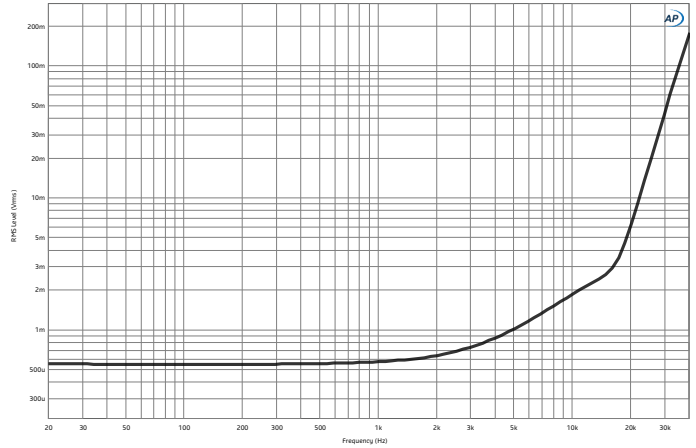
## 8 Typical Performance Graphs

Test conditions: DSA254 at 84V. Measurement bandwidth=20kHz except for small signal tests.

### 8.1 Small Signal tests

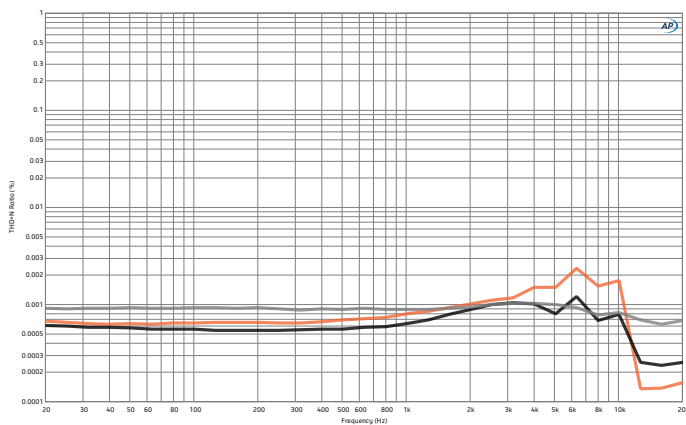


Frequency response into 2Ω (-), 4Ω (-) and 8Ω (-)

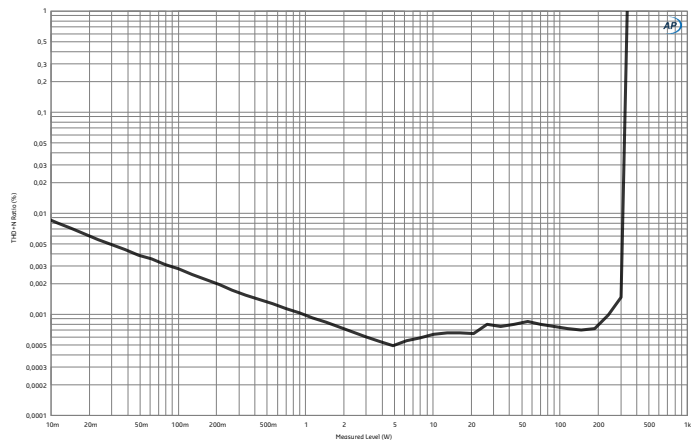


Output impedance, measured at output terminals

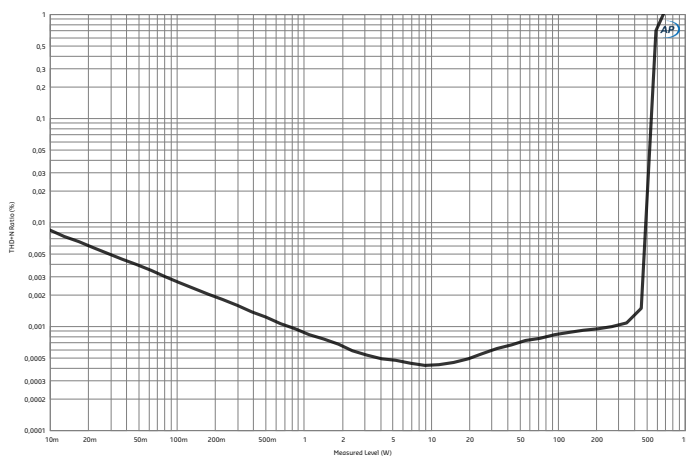
### 8.2 Large Signal Tests



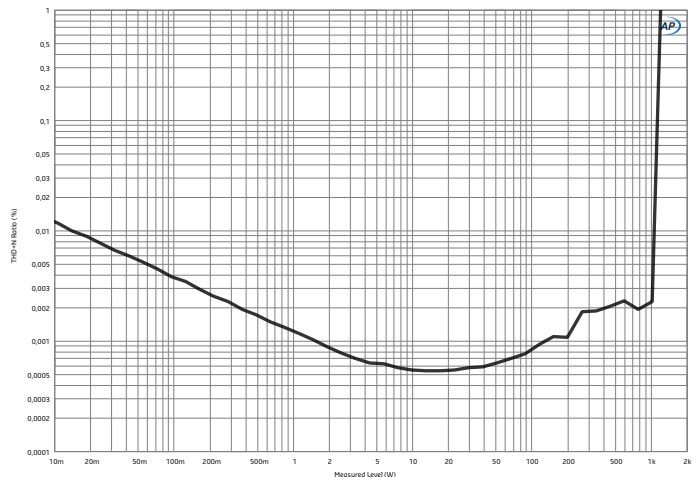
THD vs. frequency into 4Ω at 1W (-), 10W (-) and 100W (-)



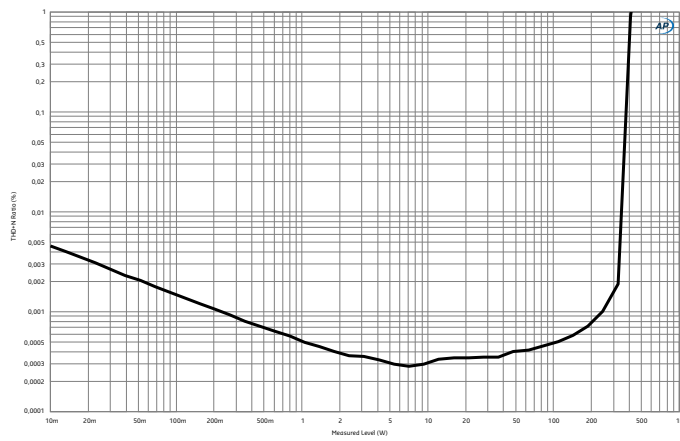
THD+N vs. power at 1kHz into 4Ω (Single Ended)



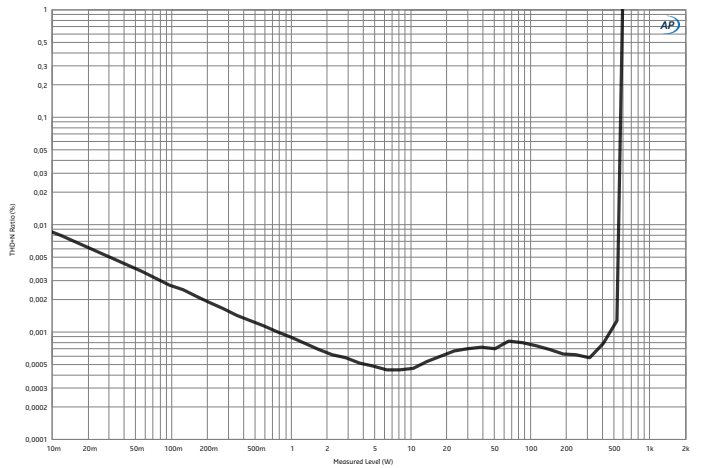
THD+N vs. power at 1kHz into 4Ω (2CH Parallel Power)



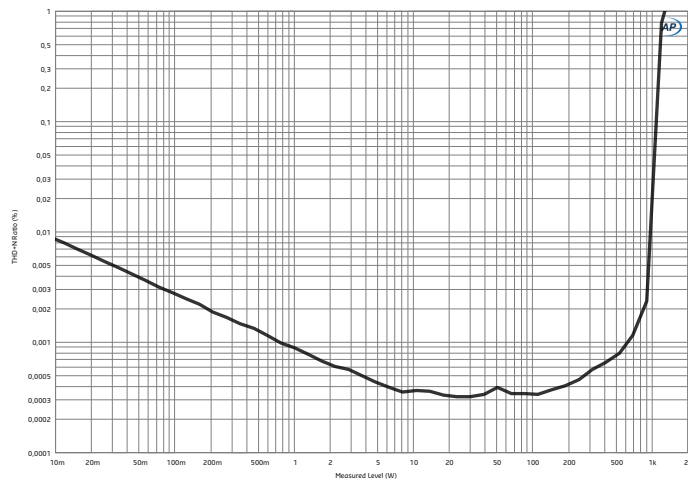
THD+N vs. power at 1kHz into 4Ω (4CH PBTL)



THD+N vs. power at 1kHz into 8Ω (Single Ended)

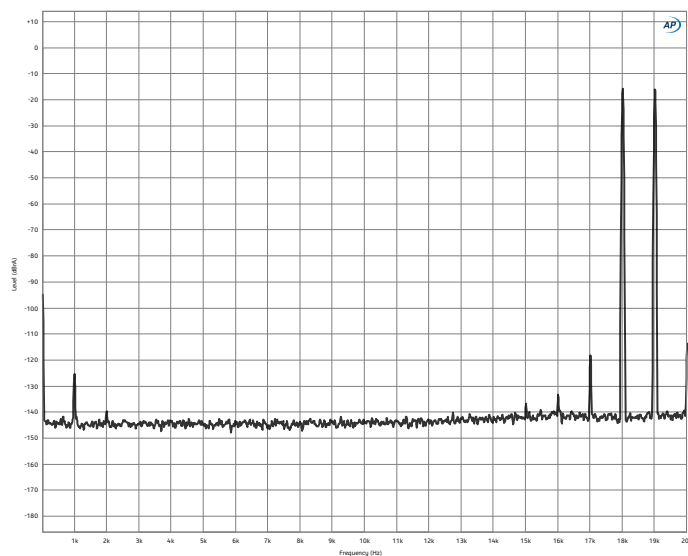


THD+N vs. power at 1kHz into 8Ω (BTL)

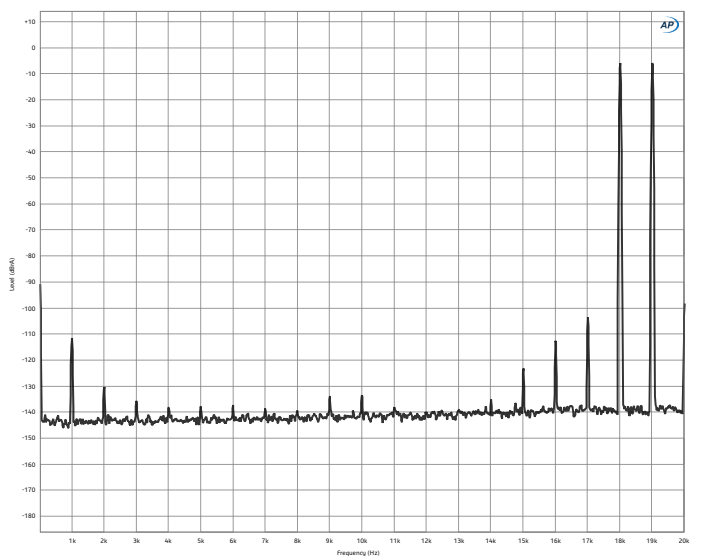


THD+N vs. power at 1kHz into 8Ω (PBTL)

### 8.3 IMD Tests (4Ω)



Noise floor and distortion residual at 5W



Noise floor and distortion residual at 50W



## 10 Revisions

Document Revision	Module Revision	Change Log	Date
R0	Proto	Preliminary	27.02.2024
R1	Proto	Connector J1 update	25.10.2024
R2	Proto	I <sup>2</sup> C registers updated	08.11.2024
R3	0-series	Performance graphs added	02.12.2024
R4	0-series	5.5 description clarified	19.12.2024
R5	0-series	Updates on Electrical -, Amplifier -, Audio IO -, Environmental specifications, I <sup>2</sup> C registers, Applications	09.07.2025

## 11 Disclaimer

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