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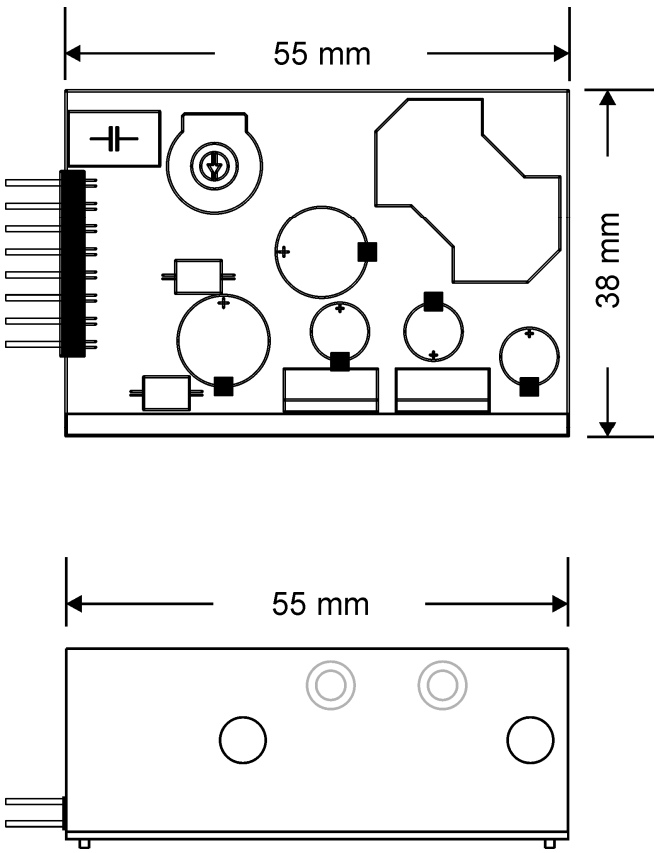
UcD180LP

High Efficiency Power Amplifier Module (Low Profile OEM Version)



Highlights

- Flat, fully load-independent frequency response
- Low output impedance
- Very low, frequency-independent THD
- Very low noise
- Fully passive loop control
- Consistent top performer in listening trials

Features

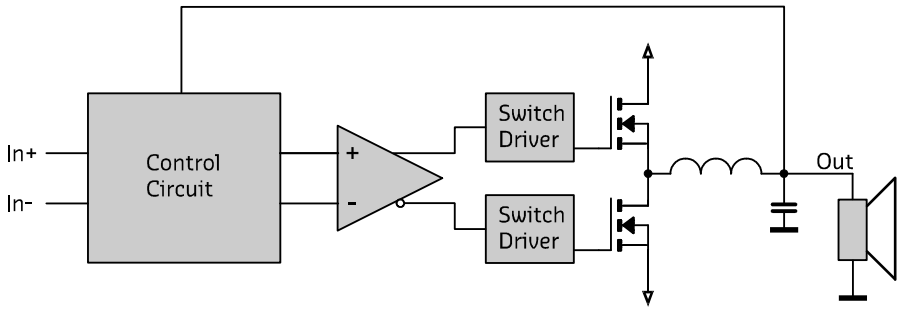
- Runs on unregulated +/- rails
- Pop-free start and stop control
- Differential audio input
- DC-fault detection
- Overcurrent and overvoltage protection
- Weight: 55 g / Height: 26mm

Applications

- Monitor loudspeakers for recording and mastering studios
- Audiophile power amplifiers for professional and consumer use
- Public Address systems
- Home theatre systems
- Active loudspeakers

Description

The UcD180LP (Low Profile Low Profile OEM version) amplifier module is a self-contained high-performance class D amplifier intended for a wide range of audio applications, ranging from Public Address systems to ultrahigh-fidelity replay systems for studio and home use. Chief distinguishing features are flat frequency response irrespective of load impedance, nearly frequency-independent distortion behaviour and very low radiated and conducted EMI. Control is based on a phase-shift controlled self-oscillating loop taking feedback only at the speaker output.



Contents

1 Performance data

Power supply = +/-45V, Load=4Ω, MBW=40kHz, Source imp=40Ω ,unless otherwise noted

Item	Symbol	Min	Typ	Max	Unit	Notes
Output Power	P_R	-	180	-	W	THD=1%, Load=4Ω
		-	120	-	W	THD=1%, Load=8Ω
Distortion	THD+N	-	0.05	0.07	%	20Hz<f<20kHz [1] Pout<P_R/2
		-	-	0.02	%	20Hz<f<20kHz Pout=1W
Output noise	U_N	-	17	25	µV	Unwtd, 20Hz-20kHz
Output Impedance	Z_{OUT}	-	-	22	mΩ	f<1kHz
		-	-	90	mΩ	f<20kHz
Power Bandwidth	PBW		20-35k		Hz	[2]
Frequency Response		DC	-	48k	Hz	+0/-3dB. All loads.
Voltage Gain total	A_V	12.8	13.1	13.3	dB	
Supply Ripple Rejection	PSRR	60	65	-	dB	Either rail, f<1kHz.
Required input level for 180W/4Ω			5.96		V	Appropriate supply voltage assumed
Efficiency	η		92		%	Full power
Idle Losses	P_0	-	2.8	3.1	W	External VDR
		-	3.6	4.0		Internal VDR
Standby Current	I_{STBY}	-	5	7	mA	Positive rail
		-	9	12		Negative rail
Current Limit		9.5	11	12	A	Hiccup mode after 80ms limiting

Note 1: At higher audio frequencies there are not enough harmonics left in the audio band to make a meaningful THD measurement. High frequency distortion is therefore determined using a 18.5kHz+19.5kHz 1:1 two-tone IMD test.
Note 2: Dielectric losses in the output capacitor limit long term (>30s) full-power bandwidth to 15kHz.

2 Audio Input Characteristics

Item	Symbol	Min	Typ	Max	Unit	Notes
Input Impedance	Z_{IN}		1.8k		Ω	Either input to ground
CM Rejection Ratio	CMRR		55		dB	All frequencies

3 Absolute maximum ratings

Correct operation at these limits is not guaranteed. Operation beyond these limits may result in irreversible damage.

Item	Symbol	Rating	Unit	Notes
Power supply voltage	V_B	+/-50	V	Shuts down when either rail exceeds 56V-60V
VDR supply voltage	V_{DR}	12.5	V	
Peak output current	$I_{OUT,P}$	11	A	Unit current-limits at 11A
Input voltage	V_{IN}	+/-12	V	Either input referenced to ground
Air Temperature	T_{AMB}	55	ºC	
Heat-sink temperature	T_{SINK}	90	ºC	User to select heat sink to insure this condition under most adverse use case

4 Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit	Notes
Power supply voltage	V_B	20[1)]	45	50[2)]	V	
VDR supply voltage	V_{DR}	12		12.5	V	Referenced to $-V_B$.
Driver supply current	I_{DR}		30		mA	
Load impedance	Z_{LOAD}	1			Ω	
Source impedance	Z_{SRC}			100	Ω	
Effective power supply storage capacitance	C_{SUP}	4700µ[3)]			F	Per rail, per attached amplifier. 4Ω load presumed.

Note 1: Reduced performance.
Note 2: Unit shuts down when either rail exceeds 56V.
Note 3: The effective power supply storage capacitance of Hypex SMPS is already in excess of 4700µF. Do not add supplementary capacitance.

5 Connections

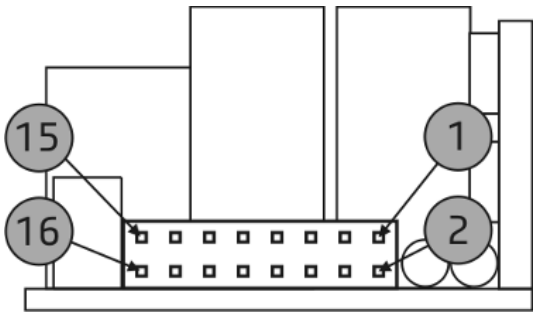


Figure 1: Connector pinning UcD180LP (Low Profile OEM version).

5.1 J1

In order to ease connecting the amplifier, all necessary connections to operate the amplifier are grouped in one standard 2.54mm pitch dual row 8 pin header.

Pin	Type	Function
1, 3	Input	Negative power supply connection
2, 4	Input	Positive power supply connection
5	Output	Amplifier ready
6	Input	Power supply ground connection[1)]
7	Input	ON/OFF control (Active low)

8	Output	DC-fault detection (Open collector - Active low)
9	Input	Non-inverting audio input
10	Input	Inverting audio input
11, 13	Output	Loudspeaker connection (hot)
12, 14	Output	Loudspeaker connection (cold)[1)]
15	Output	Current limiter monitoring.
16	Input	External driver voltage (optional).

Note 1: Pin 6,12 and 14 are physically connected to the same potential (ground).

5.2 UcD100OEM/UcD180LPOEM compatibility

In essence the UcD180LP OEM is pin compatible with the less powerful UcD100 OEM. Pin 15 and 16 of the UcD180LP OEM header must NOT be connected when fitting the amplifier into an existing UcD100 OEM setup. Pin 5 functionality will be lost because this pin will be connected to ground in a typical UcD100 OEM application which is not a problem.

5.3 DC-Error Detection Characteristics

The UcD180LP (Low Profile OEM version) has an integrated DC-error detection which will pull pin 8 low in case of such an event. It is recommended to sense this fault condition and to interrupt both power supply lines in such an event.

Item	Type	Min	Typ	Max	Unit	Notes
Voltage on pin 8, DC-error	Output			1	V	Internal open collector[1)]

Note 1: Must be pulled to a positive voltage by means of an external resistor. Open collector maximum output current: 100mA. Maximum collector voltage: 65V.

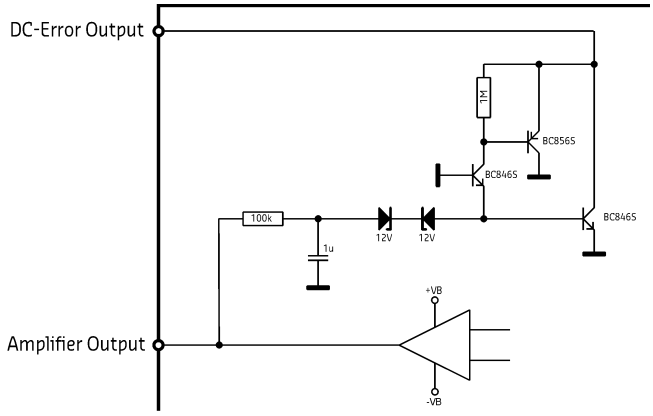


Figure 2: DC-Error Output interface.

5.4 Amplifier On/OFF Characteristics

Pulling pin 7 low enables the amplifier. Leaving pin 7 floating will put the amplifier in standby. This pin may be driven from a logical output or an open collector.

Item	Min	Typ	Max	Unit	Notes
Voltage on pin 7, left floating			3	V	Internally pulled up
Pull-up current	20		60	uA	
Threshold voltage	1.8	2.2	2.7	V	
Permissible voltage range	-5	-	75	V	

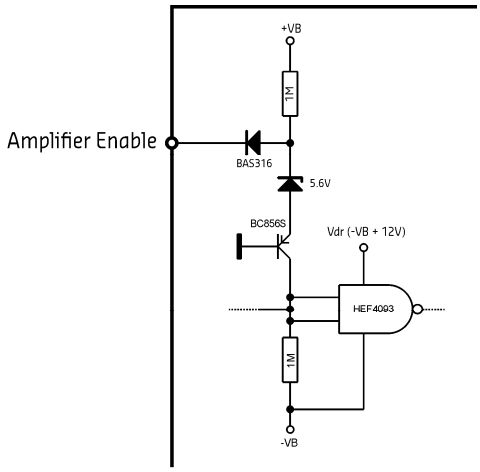


Figure 3: Amplifier On/Off Control interface.

5.5 Amplifier Ready Characteristics

Pin 5 is pulled low when the amplifier is operating normally and becomes high when the amplifier is muted or shut down due to an error such as overvoltage or overcurrent. Source and sink currents are kept low to allow clamping by the internal diodes of an attached logic input. Pin 5 may be held at or forced to any voltage between -0.6 and 5.2V without error.

Item	Min	Typ	Max	Unit	Notes
Open-circuit voltage (ready=low)	-0.6	-0.4	0	V	
Open-circuit voltage (muted=high)	4	5	5.6		
Source current (high)	20	-	60	uA	
Sink current (low)	40	-	80	uA	

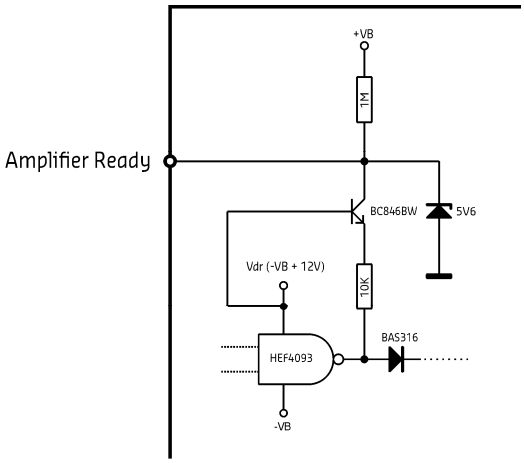


Figure 4: Amplifier Ready interface.

5.6 Current Limiter Monitoring

The current limiter monitor output is pulled low each time a switching period is cut short by current limiting. This output is not latched/delayed and produces very short pulses.

Item	Min	Typ	Max	Unit	Notes
Open-circuit voltage (limiting)	-0.6	-0.4	0	V	
Open-circuit voltage (normal)	4	5	5.6		
Source current (high)	20	-	60	uA	
Sink current (low)	140	-	180	uA	

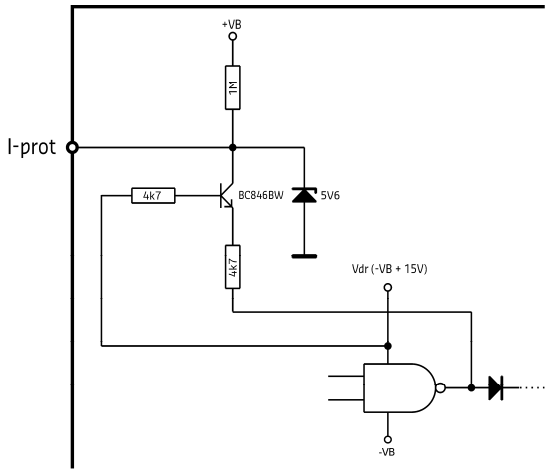


Figure 5: Current limiter monitoring.

5.7 Amplifier start-up delay

During initial power up the amplifier is disabled for approx. 1.5s regardless of the state of pin 7. Once powered up there is no start or stop delay. Pin 5 (Amplifier Ready) remains high during the initial power up.

5.8 External Driver Voltage Connection

Internal VDR supply is default set. In order to minimize dissipation in multi channel applications an external voltage source can be connected. The VDR reference must be connected to the negative supply rails(!).

Item	Min	Typ	Max	Unit	Notes
External driver voltage	11,5		12	V	1)

Note 1: Depends on board version. Contact support for additional information.

6 Input buffer recommendation

The UcD180LP (Low Profile OEM version) has no on-board input buffer. Applications that require a higher gain and/or a higher input impedance benefit from a buffer stage like shown below.

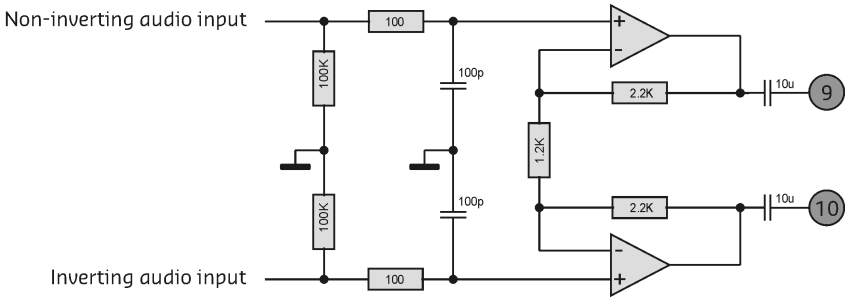
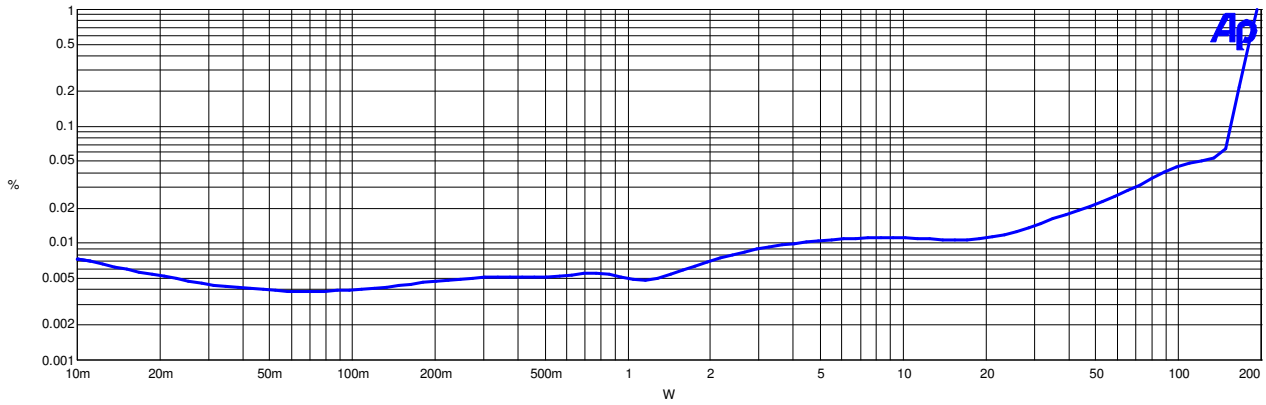


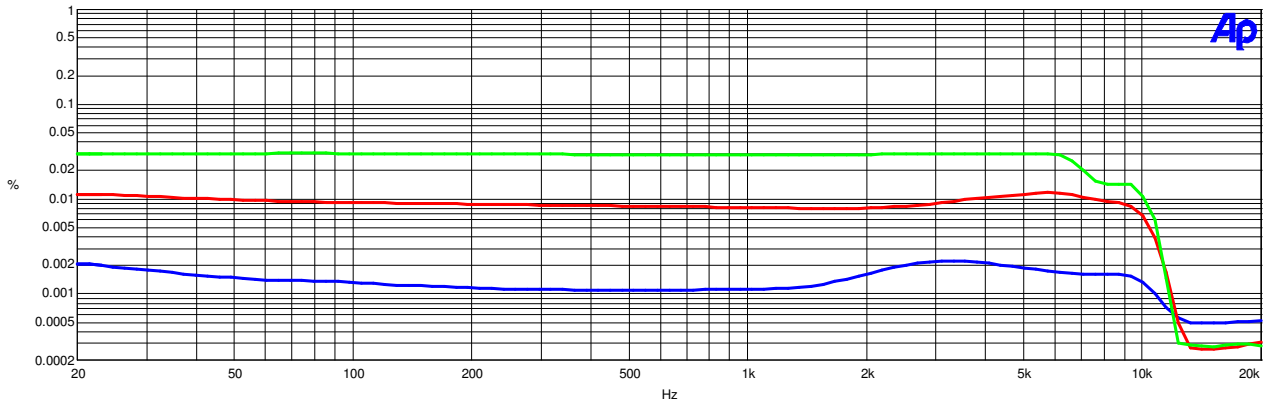
Figure 6: Recommended Input buffer stage.

7 Typical Performance Graphs

7.1 THD vs. Power (1kHz, 4Ω)

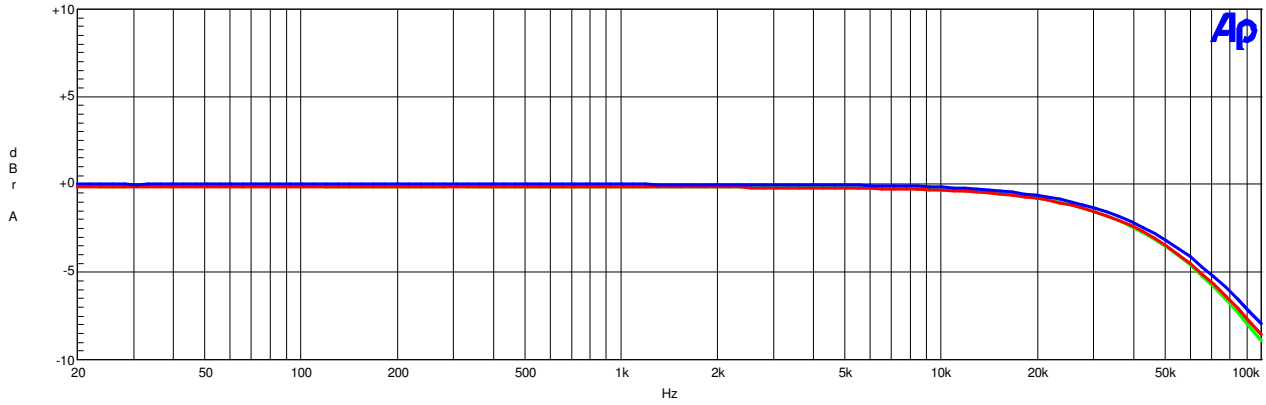


7.2 THD vs. Frequency (8Ω)



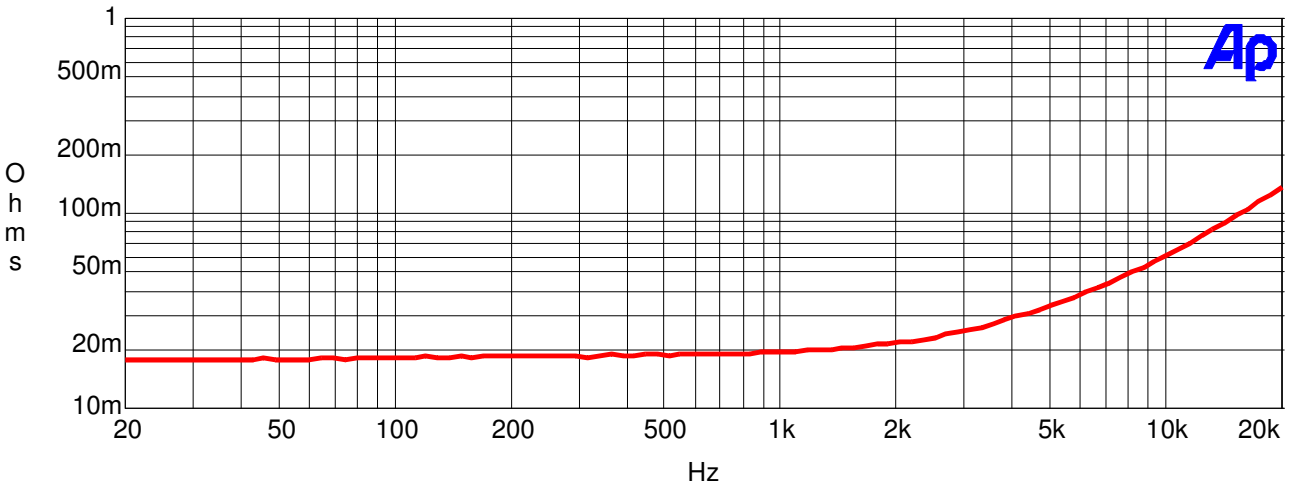
From top to bottom: 40W, 10W, 1W

7.3 Frequency Response (4Ω, 8Ω and open circuit)

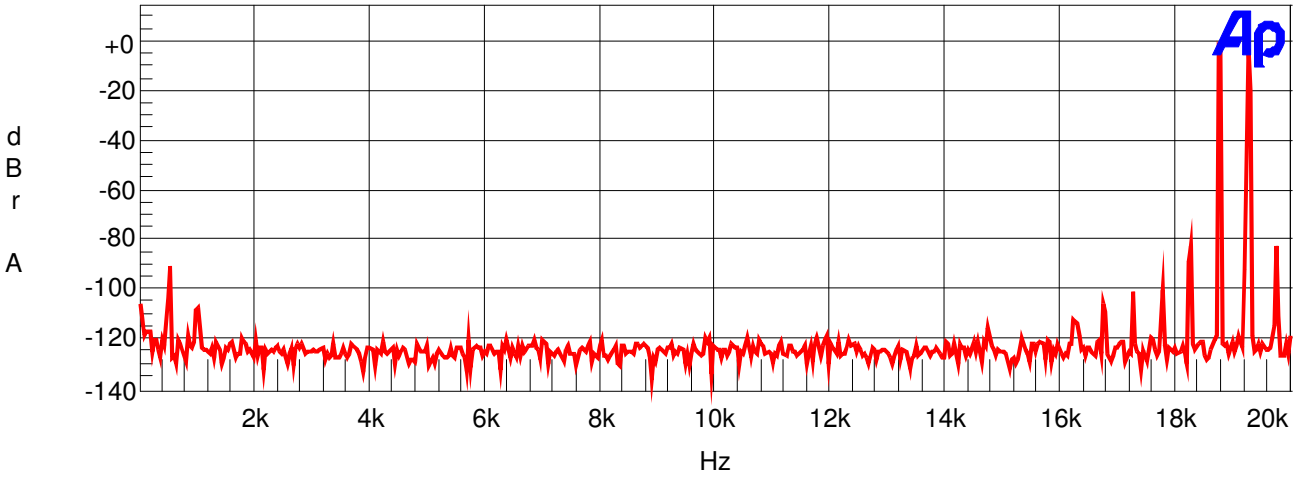


From top to bottom: open circuit, 8Ω, 4Ω

7.4 Output Impedance

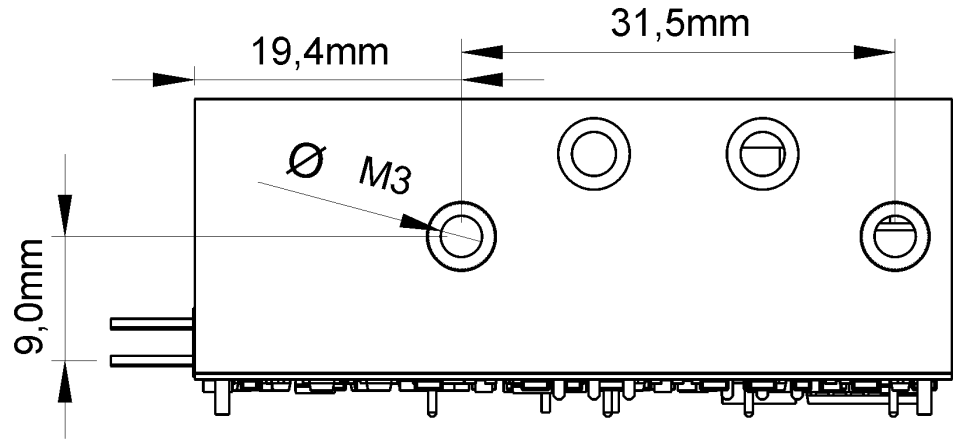


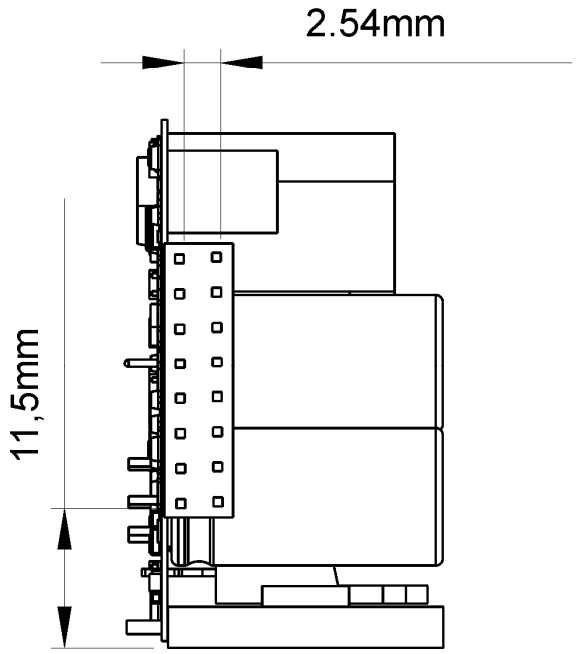
7.5 19+20kHz IMD (10W, 8Ω)



8 Connection diagram

8.1 Side view and Front view





DISCLAIMER: This subassembly is designed for use in music reproduction equipment only. No representations are made as to fitness for other uses. Except where noted otherwise any specifications given pertain to this subassembly only. Responsibility for verifying the performance, safety, reliability and compliance with legal standards of end products using this subassembly falls to the manufacturer of said end product.

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Document Revision	PCB Version	Description	Date
R1	UcD180LPOEM V1	Initial Draft.	
R2	UcD180LPOEM V2	- C7<>heatsink conflict solved. - R//RC added for improved EMI performance. - OVP protection level increased to 56V.	03.03.2009
R3	UcD180LPOEM V2	Document errors corrected: - Clip detection removed from 'Features'. - A note on page 3 wrongfully mentioned pin 5 to be GND. - Gain was corrected: 4.5dB instead of 24.5dB (previous version) for better noise.	26.06.2009
R4	UcD180LPOEM V2	- Gain typo corrected. 13dB instead of 4.5dB	24.09.2009
R5	UcD180LP OEM V3	- Current limiter monitor added. - Premature current limiting issue solved. - C7 slightly removed. - compatibility external Vdr improved. - Gain typo corrected. 13dB instead of 4.5dB - Registered Trademark symbols added.	24.09.2009
R6	UcD180LP OEM V4	- External Vdr connection improved. No more SMT component removal required. - SMT decoupling caps changed into 0805.	19.10.2009
R7	UcD180LP OEM V4	- Gain value corrected.	01.06.2010
R8	UcD180LP OEM V7	- Heat sink mounting holes moved. - Imperial push-in nuts removed from heat sink. - POWERFET's moved for better mechanics. - Improved EMI performance. - LPF DC-error modified.	07.09.2010
R9	UcD180LP OEM V8	- Over voltage protection threshold changed	10.05.2011
R10	UcD180LP OEM V8	- Recommended operating conditions updated - Format changed	25.05.2012 08.11.2012
R11	UcD180LP OEM V8	- External VDR information updated	26.05.2020
R12	UcD180LP OEM V8	- Power supply voltages/current updated	27.07.2020