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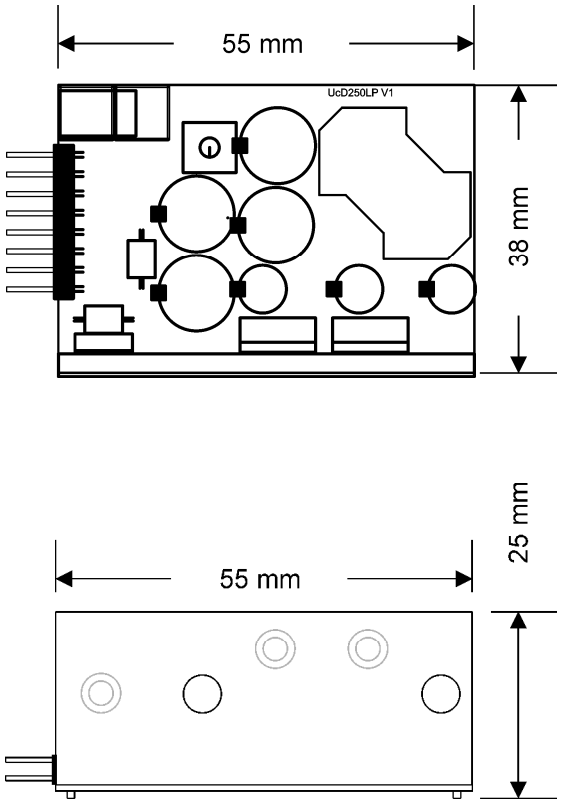
High Efficiency Power Amplifier Module (Low Profile OEM Version)



Highlights

- Flat, fully load-independent frequency response
- Low output impedance
- Very low, frequency-independent THD
- Very low noise
- Fully passive loop control
- Consistent top performer in listening trials

Features

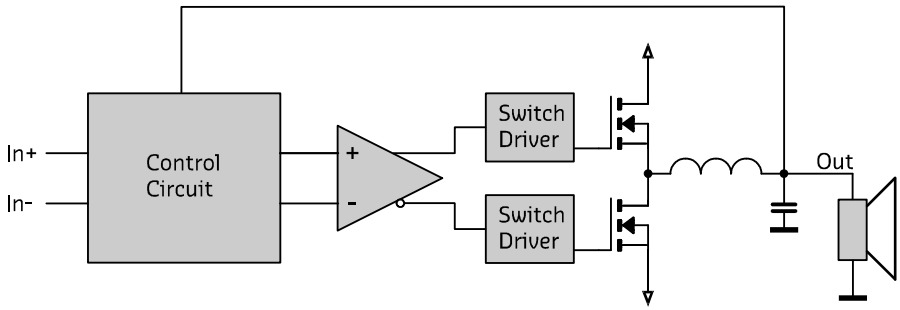
- Extended voltage headroom
- Pop-free start and stop control
- Differential audio input
- DC-fault detection
- Overcurrent and overvoltage protection
- Weight: 55 g / Height: 26mm

Applications

- Monitor loudspeakers for recording and mastering studios
- Audiophile power amplifiers for professional and consumer use
- Public Address systems
- Home theatre systems
- Active loudspeakers

Description

The UcD250LP (Low Profile Low Profile OEM version) amplifier module is a self-contained high-performance class D amplifier intended for a wide range of audio applications, ranging from Public Address systems to ultrahigh-fidelity replay systems for studio and home use. Chief distinguishing features are flat frequency response irrespective of load impedance, nearly frequency-independent distortion behaviour and very low radiated and conducted EMI. Control is based on a phase-shift controlled self-oscillating loop taking feedback only at the speaker output.



Contents

1 Performance data

Power supply = +/-64V, Load=4Ω, MBW=40kHz, Source imp=40Ω ,unless otherwise noted

Item	Symbol	Min	Typ	Max	Unit	Notes
Output Power	P_R	-	250	-	W	THD=1%, Load=4Ω
		-	180	-	W	THD=1%, Load=8Ω
Distortion	THD+N	-	0.02	0.05	%	20Hz<f<20kHz [1] Pout<P_R/2
		-	0.003	0.02	%	20Hz<f<20kHz Pout=1W
Output noise	U_N	-	20	25	µV	Unwtd, 20Hz-20kHz
Output Impedance	Z_{OUT}	-	15	22	mΩ	f<1kHz
		-	60	90	mΩ	f<20kHz
Power Bandwidth	PBW		20-35k		Hz	[2]
Frequency Response		DC	-	56k	Hz	+0/-3dB. All loads.
Voltage Gain	A_V	13	13.3	13.5	dB	
Supply Ripple Rejection	PSRR	52	58	-	dB	Either rail, f<1kHz.
Required input level for 250W/4Ω			6.84		V	Appropriate supply voltage assumed
Efficiency	η		92		%	Full power
Idle Losses	P_0	-	4.6	5.2	W	External VDR
		-	6.6	7.4		Internal VDR
Standby Current	I_{STBY}	-	8	10	mA	Positive rail
		-	12	13		Negative rail
Current Limit		12.5	15	17	A	Hiccup mode after 80ms limiting

Note 1: At higher audio frequencies there are not enough harmonics left in the audio band to make a meaningful THD measurement. High frequency distortion is therefore determined using a 18.5kHz+19.5kHz 1:1 two-tone IMD test.
Note 2: Dielectric losses in the output capacitor limit long term (>30s) full-power bandwidth to 15kHz.

2 Audio Input Characteristics

Item	Symbol	Min	Typ	Max	Unit	Notes
Input Impedance	Z_{IN}		1.8k		Ω	Either input to ground
CM Rejection Ratio	CMRR		55		dB	All frequencies

3 Absolute maximum ratings

Correct operation at these limits is not guaranteed. Operation beyond these limits may result in irreversible damage.

Item	Symbol	Rating	Unit	Notes
Power supply voltage	V_B	+/-75	V	Unit shuts down when either rail exceeds 72V
VDR supply voltage	V_{DR}	15.5	V	
Peak output current	$I_{OUT,P}$	14	A	Unit current-limits at 15A
Input voltage	V_{IN}	+/-12	V	Either input referenced to ground
Air Temperature	T_{AMB}	55	ºC	
Heat-sink temperature	T_{SINK}	90	ºC	User to select heat sink to insure this condition under most adverse use case

4 Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit	Notes
Power supply voltage	V_B	25 [1)]	60	68 [2)]	V	
VDR supply voltage	V_{DR}	15		15.5	V	Referenced to $-V_B$.
Driver supply current	I_{DR}		35		mA	
Load impedance	Z_{LOAD}	1			Ω	
Source impedance	Z_{SRC}			100	Ω	50Ω per input
Effective power supply storage capacitance	C_{SUP}	4700µ[2)]			F	Per rail, per attached amplifier. 4Ω load.
Heat-sink temperature	T_{SINK}	0		70	ºC	

Note 1: Reduced performance.
Note 2: Unit shuts down when either rail exceeds 72V.
Note 3: The effective power supply storage capacitance of Hypex SMPS is already in excess of 4700µF. Do not add supplementary capacitance.

5 Connections

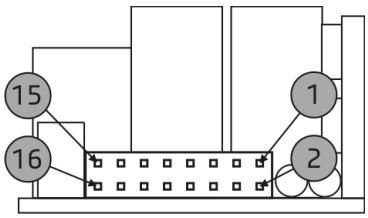


Figure 1: Connector pinning UcD250LP.

5.1 J1

In order to ease connecting the amplifier, all necessary connections to operate the amplifier are grouped in one standard 2.54mm pitch dual row 8 pin header.

Pin	Type	Function
1, 3	Input	Negative power supply connection
2, 4	Input	Positive power supply connection
5	Output	Amplifier ready
6	Input	Power supply ground connection[1)]
7	Input	ON/OFF control (Active low)
8	Output	DC-fault detection (Open collector - Active low)

9	Input	Non-inverting audio input
10	Input	Inverting audio input
11, 13	Output	Loudspeaker connection (hot)
12, 14	Output	Loudspeaker connection (cold) [1)]
15	Output	Current limiter monitoring.
16	Input	Optional External driver voltage

Note 1: Pin 6,12 and 14 are physically connected to the same potential (ground).

5.2 Heatsink connection

The heatsink of the UcD250lp is connected to ground with 2x100nF capacitors.

5.3 UcD180LP/UcD250LP/UcD400OEM compatibility

The UcD250LP OEM is pin compatible with the less powerful UcD180 OEM, but has the same supply voltage range as the UcD400OEM modules, making multiway loudspeaker design more economical.

5.4 External Driver Voltage Connection

When no external VDR is applied, the internal regulator will be used. As noted under performance data, a significant increase in idling losses is associated with this mode of operation. In order to minimize dissipation in multi channel applications an external 15V VDR source can be connected. The VDR reference must be connected to the negative supply rails(!).

5.5 DC-Error Detection Characteristics

The UcD250LP has an integrated DC-error detection which will pull pin 8 low in case of such an event. It is recommended to sense this fault condition and to interrupt both power supply lines in such an event.

Item	Type	Min	Typ	Max	Unit	Notes
Voltage on pin 8, DC-error	Output			1	V	Internal open collector[1)]

Note 1: Must be pulled to a positive voltage by means of an external resistor. Open collector maximum output current: 100mA. Maximum collector voltage: 65V.

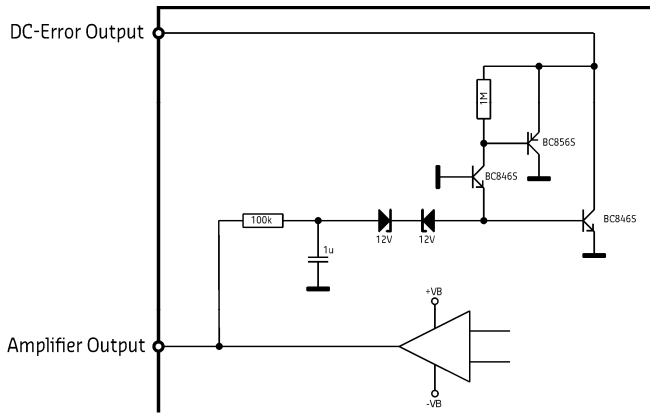


Figure 2: DC-Error Output interface.

5.6 Amplifier On/OFF Characteristics

Pulling pin 7 low enables the amplifier. Leaving pin 7 floating will put the amplifier in standby. This pin may be driven from a logical output or an open collector.

Item	Min	Typ	Max	Unit	Notes
Voltage on pin 7, left floating			3	V	Internally pulled up
Pull-up current	20		60	uA	
Threshold voltage	1.8	2.2	2.7	V	

Permissible voltage range	-5	-	75	V	

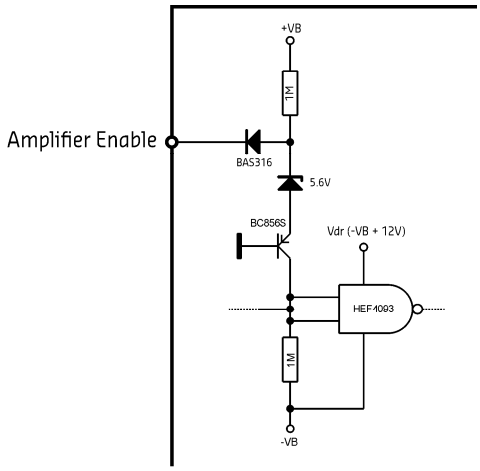


Figure 3:. Amplifier On/Off Control interface.

5.7 Amplifier Ready Characteristics

Pin 5 is pulled low when the amplifier is operating normally and becomes high when the amplifier is muted or shut down due to an error such as overvoltage or overcurrent. Source and sink currents are kept low to allow clamping by the internal diodes of an attached logic input. Pin 5 may be held at or forced to any voltage between -0.6 and 5.2V without error.

Item	Min	Typ	Max	Unit	Notes
Open-circuit voltage (ready=low)	-0.6	-0.4	0	V	
Open-circuit voltage (muted=high)	4	5	5.6		
Source current (high)	20	-	60	uA	
Sink current (low)	40	-	80	uA	

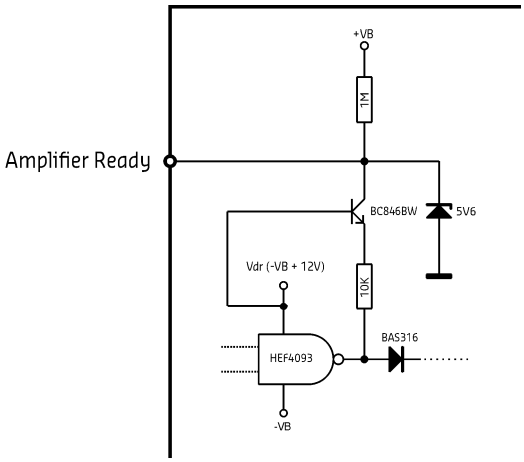


Figure 4: Amplifier Ready interface.

5.8 Current Limiter Monitoring

The current limiter monitor output is pulled low each time a switching period is cut short by current limiting. This output is not latched/delayed and produces very short pulses.

Item	Min	Typ	Max	Unit	Notes
Open-circuit voltage (limiting)	-0.6	-0.4	0	V	
Open-circuit voltage (normal)	4	5	5.6		

Source current (high)	20	-	60	uA	
Sink current (low)	140	-	180	uA	

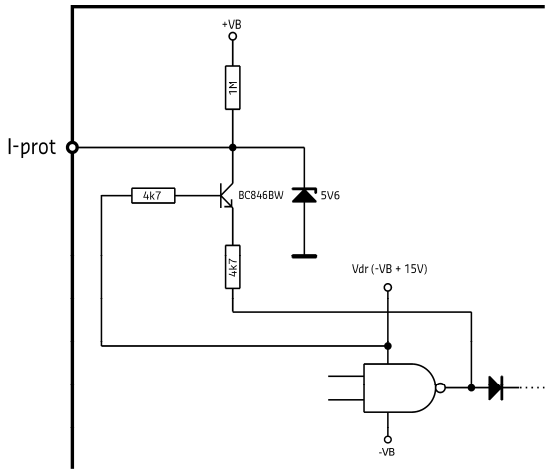


Figure 5: Current limiter monitoring.

5.9 Amplifier start-up delay

During initial power up the amplifier is disabled for approx. 1.5s regardless of the state of pin 7. Once powered up there is no start or stop delay. Pin 5 (Amplifier Ready) remains high during the initial power up.

6 Input buffer recommendation

The UcD250LP (Low Profile OEM version) has no on-board input buffer. Applications that require a higher gain and/or a higher input impedance benefit from a buffer stage like shown below.

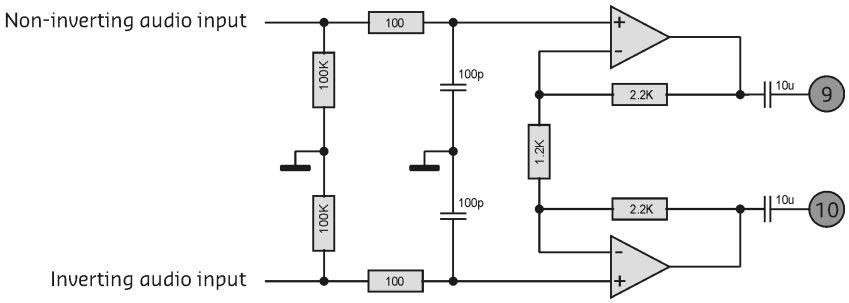
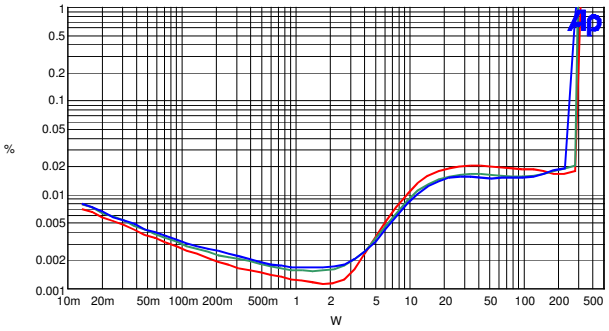
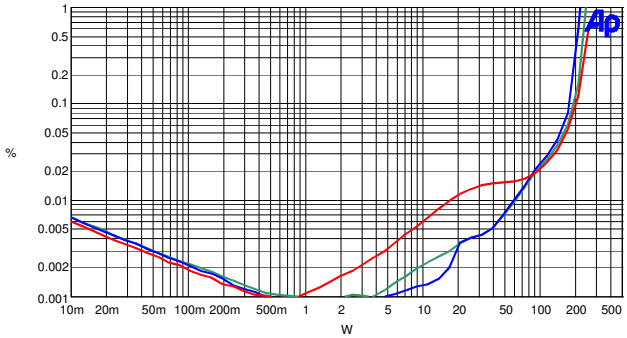


Figure 6: Recommended Input buffer stage.

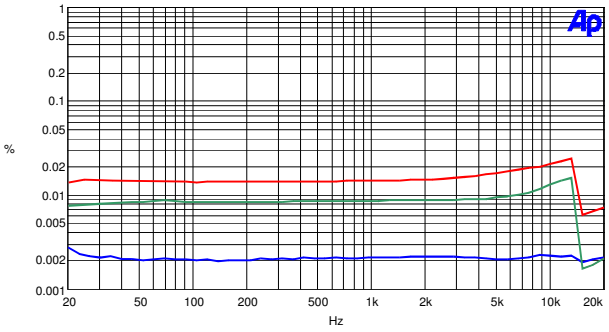
7 Typical Performance Graphs



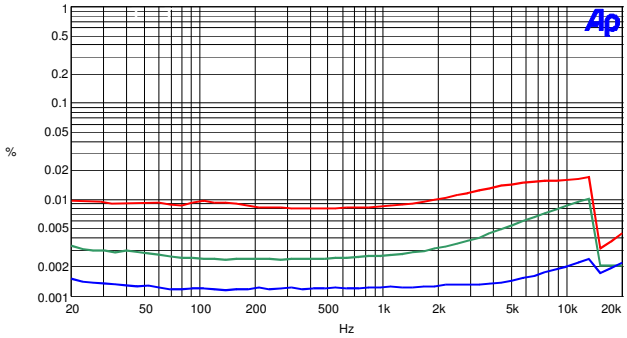
THD vs. Power (4Ω)
100Hz (blue), 1kHz (green), 6kHz (red)



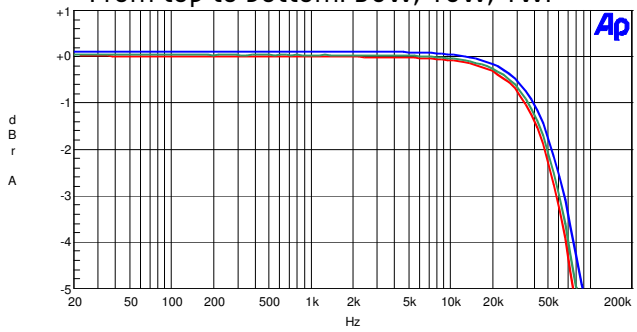
THD vs. Power (8Ω). 100Hz (blue), 1kHz (green), 6kHz (red)



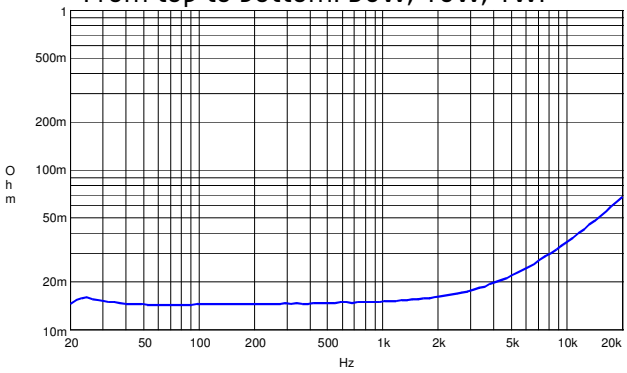
THD vs. Frequency (4Ω)
From top to bottom: 50W, 10W, 1W.



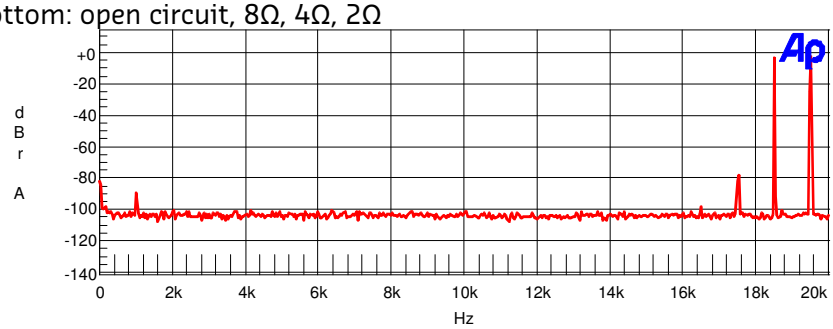
THD vs. Frequency (8Ω)
From top to bottom: 50W, 10W, 1W.



Frequency Response
From top to bottom: open circuit, 8Ω, 4Ω, 2Ω



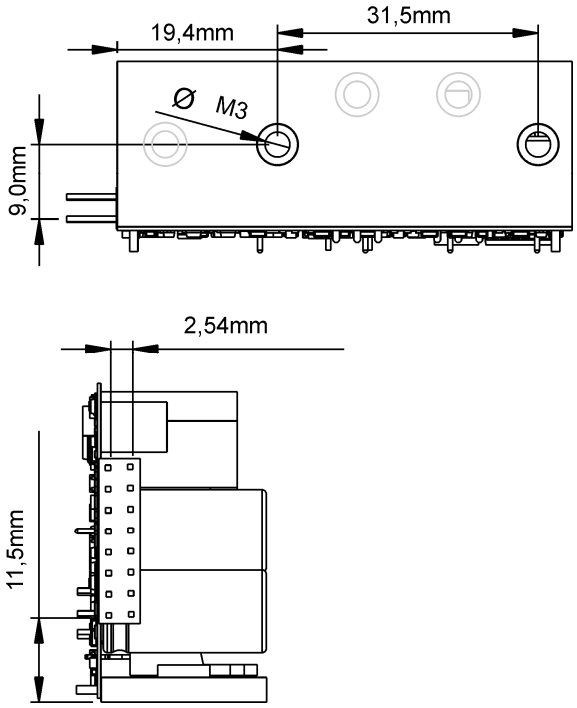
Output Impedance



IMD spectrum
(18.5kHz + 19.5kHz, 10W, 4Ω)

8 Connector layout

8.1 Front view and Side view



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Document Revision	PCB Version	Description	Date
R1	UcD250LPOEM V1	Initial Draft.	01.11.2010
R2	UcD250LPOEM V1	Recommended heat sink temperature added.	13.01.2011
R3	UcD250LPOEM V1	Heat sink height corrected (page1).	28.04.2011
R4	UcD250LPOEM V2	Recommended operating conditions updated Format changed	25.05.2012 08.11.2012
R5	UcD250LPOEM V3	Heatsink connection changed and information updated	01.11.2013
R6	UcD250LPOEM V3	Typo in R5 PCB version, changed from V2 to V3	27.03.2018
R7	UcD250LPOEM V3	External VDR information updated	29.07.2020